ERJ
Engineering Research Journal
Faculty of Engineering
Minoufiya University

A GENETIC ALGORITHM APPROACH TO MINIMIZE THE TOTAL HARMONIC DISTORTION OF THE MULTILEVEL INVERTER

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ABSTRACT

This paper presents a genetic algorithm (GA) optimization technique to determine the optimum switching angles of the multilevel inverter. This technique is used to eliminate low order harmonics of output voltage to minimize the total harmonic distortion (THD), with different levels of configurations. The effectiveness of this technique is tested by simulation results, which are used for calculating the optimum switching angles of three-phase 11-level inverters, with equal and unequal DC supplies. Finally, the results show that the GA technique gives lower THD compared with results reported in the literatures using other techniques.

يقدم هذا البحث استخدام تقنية خوارزمات الجينات الو راثية لتحديد زوايا الإشعال المثلي للجيل الجديد من عواكس القدرة متعددة المستوي. هذه التقنية تستخدم لحذف توافقيات الدرجة الأقل من جهد الخرج لتقليل معامل التشويه الكلي. يتم تطبيق هذا الأسلوب لتحديد زوايا الإشعال المثلي لعاكس قدرة ثلاثي الأوجه ذو احدي عشر مستوي من الخرج في حالتي تساوي وعدم تساوي جهد الدخل المستمر. توضح النتائج أن هذا الأسلوب يعطي أقل معامل تشويه كلي مقارنتا بالطرق الأخرى.

Keywords: Genetic algorithms; multilevel inverters; total harmonic distortion

1. INTRODUCTION

A multilevel inverter can be built to synthesize a desired AC voltage from several levels of DC voltages. The multilevel inverter is ideal for connecting DC energy sources (solar cells, fuel cells, and the rectified output of wind turbines) to an existing AC power grid [1]. A family of multilevel inverters have emerged as a solution for working with higher voltage levels, up to 6.9 KV [2-4]. The main advantages of multilevel inverters are their lower switching frequency compared to traditional inverters, which means they reduce the switching losses. Besides, the output waveforms of multilevel inverters are in a stepped form; therefore they have lower harmonics and lower dv/dt, compared to a square wave inverter [5].There are three main types of multilevel inverters: 1) diode-clamped inverters, 2) flying capacitor inverters and, 3) cascaded H-bridge inverters. Among these inverter topologies, the flying capacitor inverter is difficult to realize because each capacitor must be charged with a different voltage as the voltage level increases. Moreover, the diode-clamped inverter is difficult to be expanded to multilevel because of the natural problem of the DC link voltage unbalancing, the increase in the number of clamping diodes, and the difficulty of the disposition between the DC link capacitors and the devices as the voltage increases. Though the cascaded inverter has the disadvantage of separate DC sources, the modularized circuit layout and package are possible, and the problem of the DC link voltage unbalancing does not exist. Therefore, it is easily expanded to multilevel configuration. The main disadvantages associated with the multilevel inverter are its circuit complexity, requirement of a high number of power switches that must be commutated in a precisely determined sequence by a dedicated (and complex) modulator circuit. Because of these disadvantages of old configurations, a recent topology of multilevel inverter is used in this work [6, 7].

2. RECENT TOPOLOGY OF MULTILEVEL INVERTERS

The main purpose of the recent family of multilevel inverters is to reduce the number of switching devices used without changing the staircase nature of the output voltage. Therefore, it should have the same number of levels [6, 7]. The simplest circuit of this family is the 5-level inverter that shown in Fig.1.

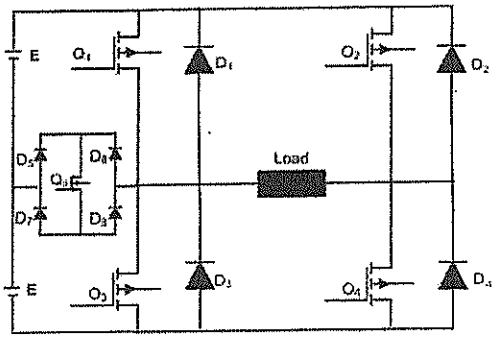

Fig.1 Simplified 5-Level Inverter.

The 5-level multilevel inverter has a main H-bridge inverter Q_1–Q_4, auxiliary switches Q_5 and two DC supplies. The function of the auxiliary switch is to control the connection of the DC supplies so as to construct the staircase output voltage. Table 1 lists the switching combinations that generate the required five output levels (E, 2E, 0, -E, -2E).

Table.1 Switching States for 5-Level Inverter.

V_L	Q_1	Q_2	Q_3	Q_4	Q_5
E	off	off	Off	on	on
2E	on	off	Off	on	off
0	off	off	On	on	off
-E	off	on	Off	off	on
-2E	off	on	On	off	off

Figure 2 shows a three-phase 11-level inverter of this family. Each phase consists of main H-bridge, four auxiliary switches and five DC supplies.

Table 2 illustrates the comparison between different multilevel inverters configuration according to numbers of main power switches as a function of number of output levels per phase, m.

The reduction of the number of switching devices in each phase of these inverters can be achieved by the following equation:

$$\{1-\frac{4+(m-3)/2}{2(m-1)}\} \qquad (1)$$

For example, the reduction in the number of the main power switches required in 11-level inverter (m=11) is 60%. (8 against 20 in any of the other three configurations).

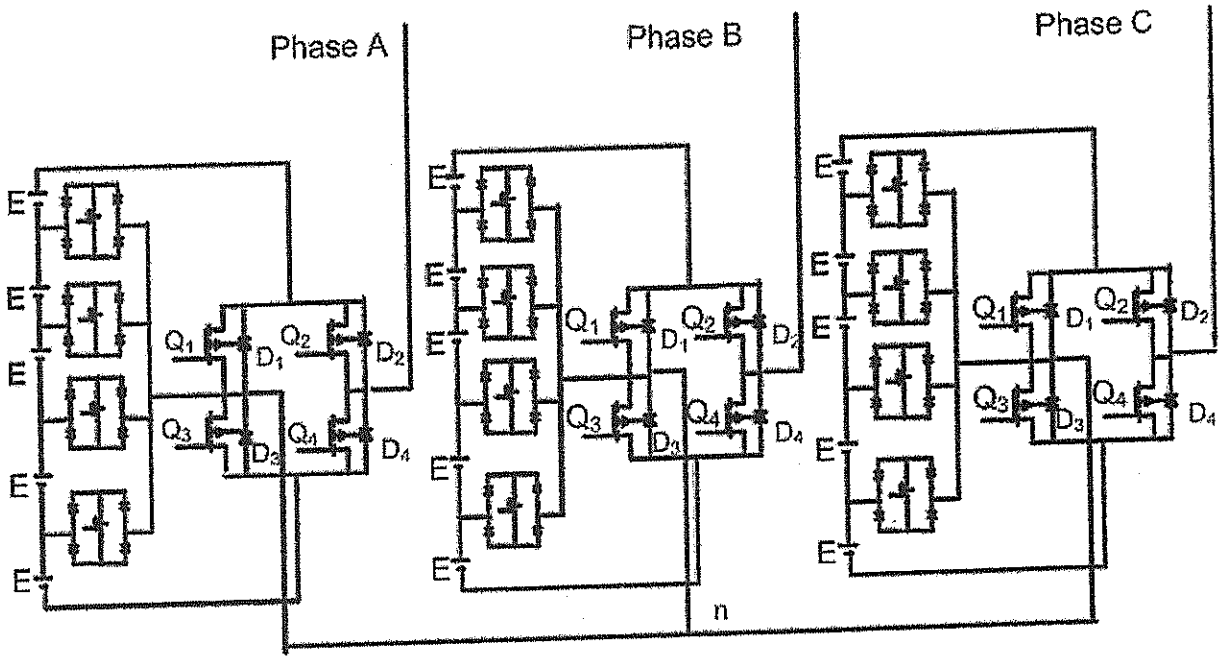

Fig.2 Simplified Three-Phase 11- Level Inverter

Table 2 Comparison between multilevel inverter types according of switches numbers

Inverter Configuration	Diode-Clamp	Capacitor-Clamp	Cascaded H-bridge	Recent Topology
Main switching devices	2 (m-1)	2 (m-1)	2 (m-1)	4+(m-3)/2
Main diodes	2 (m-1)	2(m-1)	2 (m-1)	2 (m-1)
Clamping diodes	(m-1) (m-2)	0	0	0
DC bus capacitors	(m-1)	(m-1)	(m-1)/2	(m-1)/2
Balancing capacitors	0	(m-1) (m-2)/2	0	0

3. MATHEMATICAL MODEL OF SWITCHING FOR THE MULTI-LEVEL INVERTER

The multilevel inverters use several DC sources to synthesize a sinusoidal wave. Thus, the control of the multilevel inverter is to choose a series of switching angles to synthesize a desired sinusoidal voltage waveform. Figure 3 shows a generalized quarter wave symmetric stepped voltage waveform synthesized by 2S+1 level inverter. Where S is the number of switching angles, which also equal to the number of DC sources.

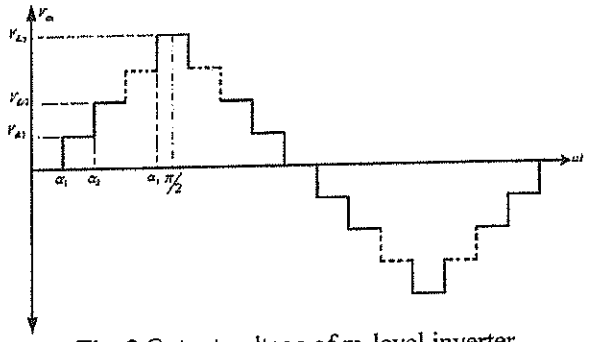

Fig. 3 Output voltage of m-level inverter

The Fourier series expansion of the (stepped) output voltage waveform of the multilevel inverter shown in Fig. 3 is given as:

$$v_0(t) = a_0 + \sum_{n=1}^{\infty}\left(a_n \cos n\omega t + b_n \sin n\omega t\right) \qquad (2)$$

Due to the odd quarter-wave symmetric characteristic, illustrated in Fig. 3, the Fourier series coefficients are given by.

$$a_0 = \frac{1}{T}\int_0^T v_0(t)\, dt = 0$$

$$a_n = \frac{2}{T}\int_0^T v_o(t)\cos(nwt)\, dt = 0$$

$$b_n = \frac{2}{T}\int_0^T v_o(t)\sin(nwt)\, dt$$

$$v_0(t) = \frac{4}{n\pi}\sum_{n=1,3,5,..}^{\infty}\left[V_{dc1}\cos(n\alpha_1) + ... + V_{dcs}\cos(n\alpha_s)\right]\sin(nwt)$$

$$b_n = \frac{4}{n\pi}\left[V_{dc1}\cos(n\alpha_1) + ... + V_{dcs}\cos(n\alpha_s)\right],\ n = 1,3,5,...$$

$$b_n = o,\ n = 2,4,6,...$$

$$v_o(t) = \frac{4}{n\pi}\sum_{n=1,3,5,..}^{\infty}\left[V_{dc1}\cos(n\alpha_1) + .. + V_{dcs}\cos(n\alpha_s)\right]\sin(nwt) \qquad (3)$$

4. CONTROL TECHNIQUES USED FOR THE MULTILEVEL INVERTER

The modulation methods used in multilevel inverters can be classified according to switching frequency (low switching frequency and high switching frequency) [8,9]. High switching frequency inverters have many commutations for the power semiconductor devices in one period of the fundamental output voltage. The popular methods in industrial applications are the classic carrier-based sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHEPWM) and space vector PWM (SVPWM) [10-12]. These techniques increase the control complexity and the switching losses. Low switching frequency inverters, generally perform one or two commutations of the power semiconductor devices during each cycle of the output voltage, to generate a staircase waveform. Representatives of this family are the multilevel selective harmonic elimination, and Space vector control [13-14].

Applying the harmonics elimination technique method, 'S-1' lowest odd harmonics can be eliminated from the single-phase output voltage. In a three-phase system, the triplen harmonics do not exist in line voltages; therefore, the 'S-1' non-triplen harmonics need to be eliminated from the line voltages. For the three-phase 11-level inverters, 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics should be eliminated. The fundamental component and the harmonics to be eliminated are given in Equations (4) through (15) for equal and unequal DC sources.

Case 1: <u>For Equal DC Sources</u>

$$V_{dc1} = V_{dc2} = ... = V_{dcs} = E$$

$$V_1 = \frac{4E}{\pi}(\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) + \cos(\alpha_5))$$

Put $m_a = \dfrac{V_1\pi}{4E}$

$M = m_a / s$

where, M is the modulation index and V_1 is the amplitude of the output voltage at the fundamental frequency.

$$m_a = \cos(\alpha_1) + \cos(\alpha_2) + ... + \cos(\alpha_5) \qquad (4)$$

$$0 = \cos(5\alpha_1) + \cos(5\alpha_2) + ... + \cos(5\alpha_5) \qquad (5)$$

$$0 = \cos(7\alpha_1) + \cos(7\alpha_2) + ... + \cos(7\alpha_5) \qquad (6)$$

$$0 = \cos(11\alpha_1) + \cos(11\alpha_2) + ... + \cos(11\alpha_5) \qquad (7)$$

$$0 = \cos(13\alpha_1) + \cos(13\alpha_2) + ... + \cos(13\alpha_5) \qquad (8)$$

The total harmonic distortion of the line voltage is:

$$THD = \frac{\sqrt{\sum_{n=5,7,...}^{\infty} V_n^{\,2}}}{V_1}$$

$$THD = \frac{\sqrt{\sum_{n=5,7,11,...}^{\infty}\left[\frac{1}{n}\left(\cos(n\alpha_1) + ... + \cos(n\alpha_5)\right)\right]^2}}{\cos(\alpha_1) + ... + \cos(\alpha_5)} \qquad (9)$$

Case 2: For Unequal DC Sources

$$v_{dc1}=K_1E,\quad v_{dc2}=K_2E,\ldots\ldots\ldots\quad v_{dcs}=K_sE$$

$$v_o(t)=\frac{4E}{n\pi}\sum_{n=1,3,5,\ldots}^{\infty}[K_1\cos(n\alpha_1)+\ldots+K_s\cos(n\alpha_s)]\sin(nwt) \quad (10)$$

$$m_a=k_1\cos(\alpha_1)+k_2\cos(\alpha_2)+\ldots\ldots\ldots+k_5\cos(\alpha_5) \quad (11)$$

$$0=k_1\cos(5\alpha_1)+k_2\cos(5\alpha_2)+\ldots\ldots\ldots+k_5\cos(5\alpha_5) \quad (12)$$

$$0=k_1\cos(7\alpha_1)+k_2\cos(7\alpha_2)+\ldots\ldots\ldots+k_5\cos(7\alpha_5) \quad (13)$$

$$0=k_1\cos(11\alpha_1)+k_2\cos(11\alpha_2)+\ldots\ldots\ldots+k_5\cos(11\alpha_5) \quad (14)$$

$$0=k_1\cos(13\alpha_1)+k_2\cos(13\alpha_2)+\ldots\ldots\ldots+k_5\cos(13\alpha_5) \quad (15)$$

The above nonlinear equations can be solved by Newton-Raphson method. This method gives one solution which depends on the initial values of switching angles. The resultant theory [15] is applied to give all solutions. The later approach uses polynomials of 22nd degree, for 7-level inverter, which is difficult and time consuming for solution process. For any changes in configuration levels or input DC voltages, a new expressions must be deduced which complicates the solution process. In this paper, a genetic algorithm (GA) optimization technique is applied to determine the optimum switching angles of the proposed topology multilevel inverters, in order to minimize the total harmonic distortion (THD). The Genetic-algorithm (GA) is used for any number of levels without extensive derivation of analytical expressions.

5. GENETIC ALGORITHMS-BASED METHOD

Genetic algorithm is a computational model that solves optimization problems by imitating genetic processes and the theory of evolution. It imitates biological evolution by using genetic operators like reproduction, crossover, mutation, etc [16].

Optimization in GA means maximization or minimization. In this case, minimization technique is required. There are only few parameters to be set for GA to work. The steps for formulating a problem and applying GA are as follows:

1- Select binary or floating-point strings.

2- Find the number of variables specific to the problem; these numbers will be the numbers of genes in a chromosome. In this application, the number of variables is the number of controllable switching angles. The 11-level inverter requires five DC sources per phase; thus, each chromosome for this application will have five switching angles, i.e. $\{\alpha_1, \alpha_2, \alpha_3, \alpha_4, \alpha_5\}$.

3- Set a population size and initialize the population. In this application a population size of 20 is selected. The selection of optimum-sized population requires some experience in GA. The population in this paper has 20 chromosomes, each containing five switching angles. The population is initialized with random angles between 0 and 90 degrees.

4-The most important item for the GA to evaluate the fitness of each chromosome is the cost function. The objective of this study is to eliminate the low order harmonics in order to minimize the total harmonic distortion THD.

5- GA is usually set to run for a maximum number of iterations (1000 in this case) to obtain one answer.

Note that: after these iterations, GA evaluates one optimal solution. A MATLAB m-file is designed program is built to solve this problem for any number of inverter levels. The main implementation steps of the GA-based optimisation are summarized in the flowchart shown in Fig. 4. The GA method for three-phase 11-level inverter is used with equal and unequal DC sources, at a modulation index from 0.2 to 1.0.

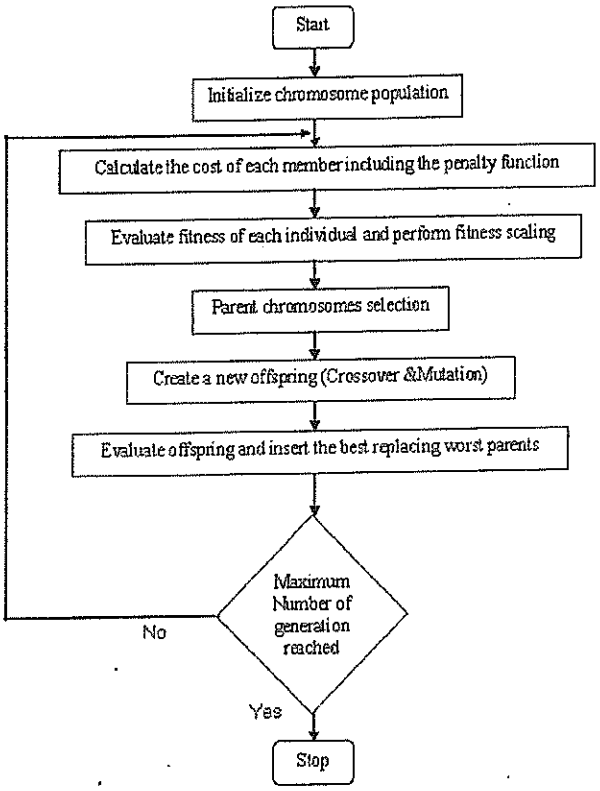

Fig. 4. Flowchart of the GA evolution process

Figure 5 shows the optimal switching angles versus m_a for three-phase 11-level inverter, while Fig. 6 shows the line voltage THD versus m_a for three-phase 11-level inverter for equal DC sources. Figure 7 shows the optimal switching angles versus m_a for three-phase 11-level inverter, while Fig. 8 shows the line voltage THD versus m_a for three-phase 11-level inverter for unequal DC sources. For poth cases the consitran ($\alpha_1<\alpha_2<\alpha_3<\alpha_4<\alpha_5<90$) is satisfied.

Figure 9 Shows that the value of total harmonic distortion THD for Genetic algorithm-based method is lower than the SPWM and harmonic elimination using *Newton-Raphson* methods at all value of modulation index (M)

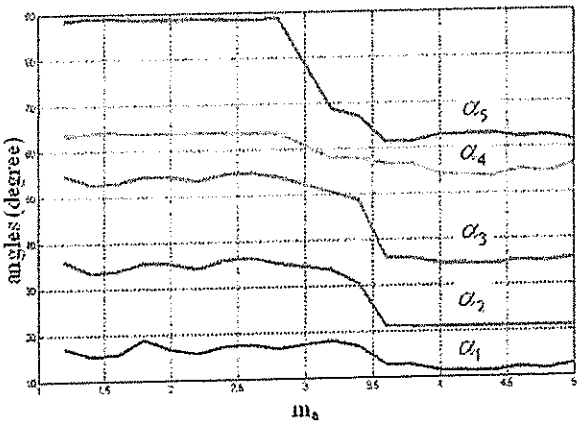

Fig.5 The optimal switching angles versus m_a for three-phase 11-level inverter with equal DC sources using GA.

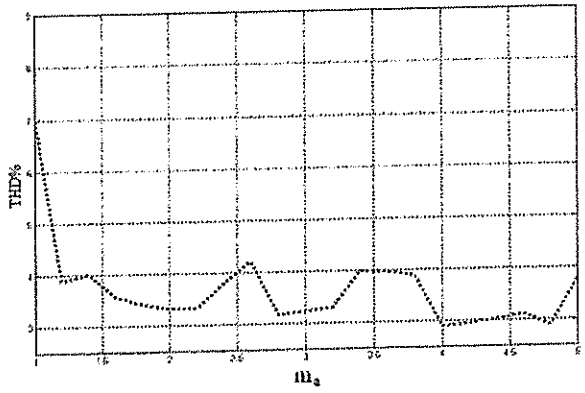

Fig. 6. line voltage THD versus m_a for three-phase 11-level inverter with equal DC sources.

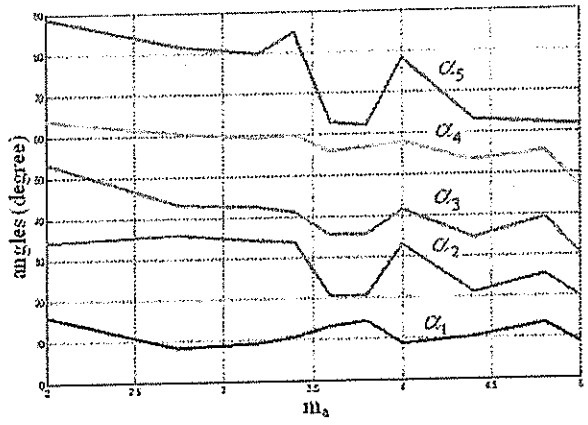

Fig.7 The optimal switching angles versus m_a for three-phase 11-level inverter with unequal DC sources using GA.

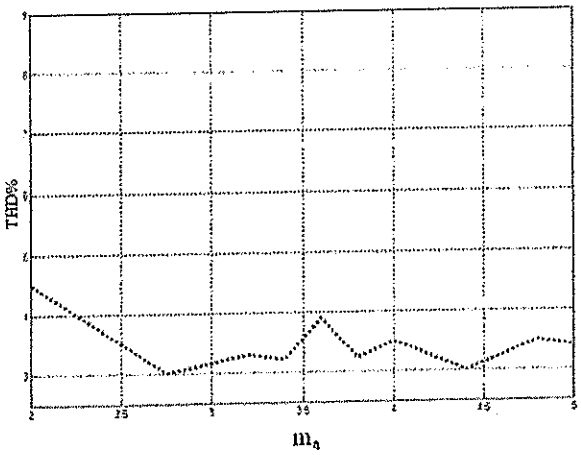

Fig. 8. Line voltage THD versus m_a for three-phase 11-level inverter with unequal DC sources.

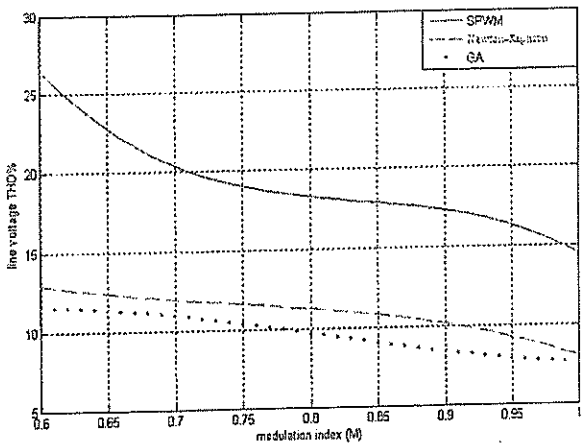

Fig 9.line voltage THD versus modulation index M for three-phase 7-level inverter for PWM, harmonic elimination using Newton-Raphson and Genetic algorithm methods

6. SIMULATION RESULTS FOR EQUAL DC SOURCES INVERTERS

A simulation program has been developed using the MATLAB package to investigate the performance of three-phase 11-level inverter with equal DC sources. The load is assumed as a static RL load with 100 Ω resistor and 255 mH reactor, while the DC supplies are equals with 70 V as case study. The investigations are carried out for two values of the modulation index (M) 0.80 and 0.65 as case study. The results of the simulation are illustrated in Figs. 10 through 13. The Fast Fourier Transform (FFT) is used to analyze the output line voltages.

Note that the harmonic content of the current is significantly reduced compared to the harmonic content of the output voltage due to the filtering effect of the load inductance.

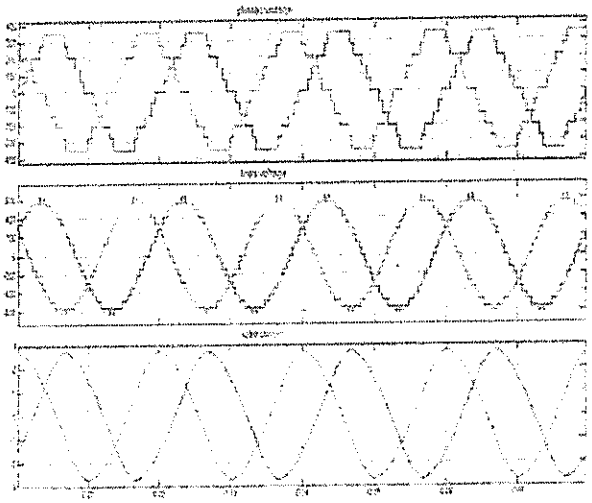

Fig. 10 Simulation waveforms for three-phase 11-level inverter at M=0.80 using GA.

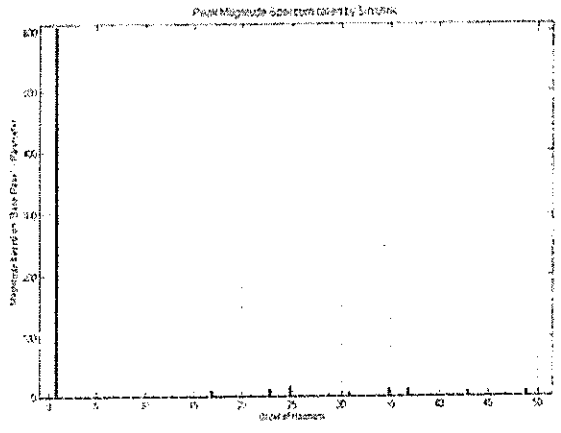

Fig. 11. FFT of the line voltage for three-phase 11-level inverter at M=0.80 using GA.

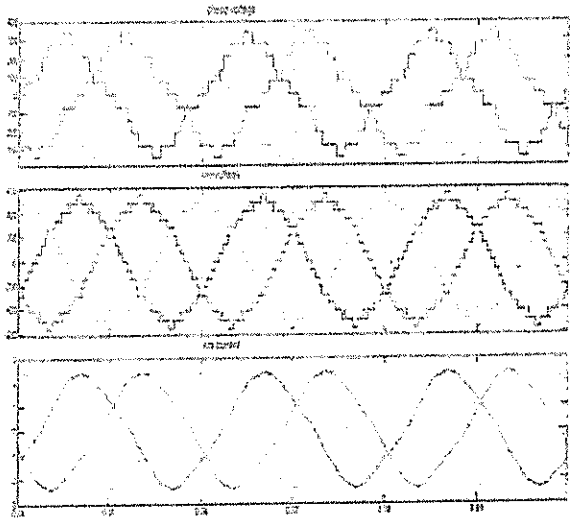

Fig. 12 Simulation waveforms for three-phase 11-level inverter at M=0.65 using GA.

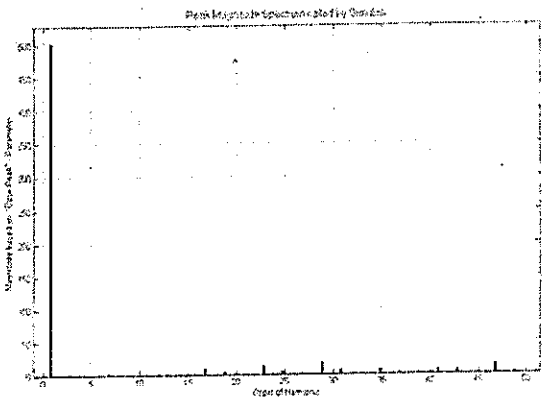

Fig. 13. FFT of the out put voltage for three-phase 11-level inverter at M=0.65 using GA.

7. SIMULATION RESULTS FOR UNEQUAL DC SOURCES INVERTER

A simulation program has been developed using the MATLAB package to investigate the performance of the three-phase 11-level inverter with unequal DC sources. The load is assumed as a static RL load with 100 Ω resistor and 255 mH reactor and E = 70 V as case study. The investigations are carried out for two values of the modulation index (M) 0.80 and 0.65 as case study.

For M = 0.8, $k_1 = 1.086$, $V_{dc1} = 76.02V$, $k_2 = 1.1223$, $V_{dc2} = 78.561V$, $k_3 = 1.0309$, $V_{dc3} = 72.163V$, $k_4 = 0.9665$, $V_{dc4} = 67.655V$ and $k_5 = 1.0004$, $V_{dc5} = 70.028V$.

For M = 0.65, $k_1 = 1.1378$, $V_{dc1} = 79.646V$, $k_2 = 0.9366$, $V_{dc2} = 65.562V$, $k_3 = 0.8955$, $V_{dc3} = 62.685V$, $k_4 = 1.104$, $V_{dc4} = 77.28V$ and $k_5 = 1.0728$, $V_{dc5} = 75.096V$.

The results of the simulation are illustrated in Figs. 14 through 17. The Fast Fourier Transform (FFT) is used to analyse the output line voltage.

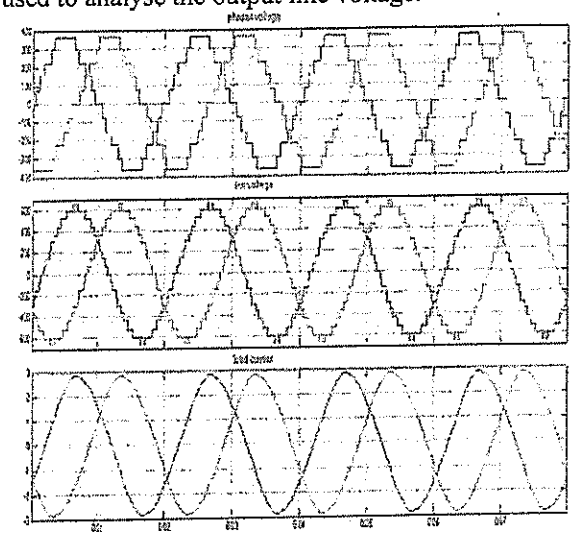

Fig. 14 Simulation waveforms for three-phase 11-level inverter unequal DC source at M=0.80 using GA.

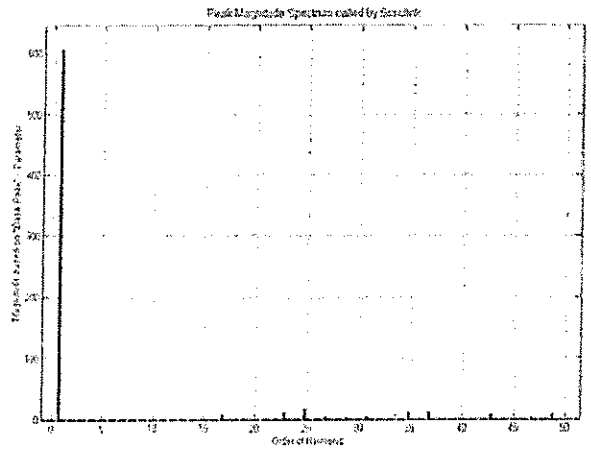

Fig. 15 FFT of the out put voltage for three-phase 11-level unequal DC source inverter at M=0.8 using GA.

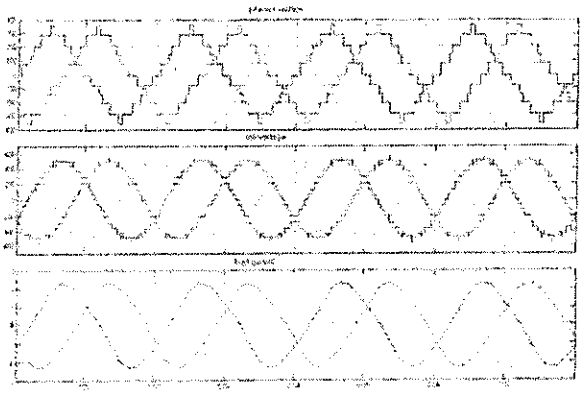

Fig. 16. Simulation waveforms for three-phase 11-level inverter unequal DC source at M=0.65 using GA.

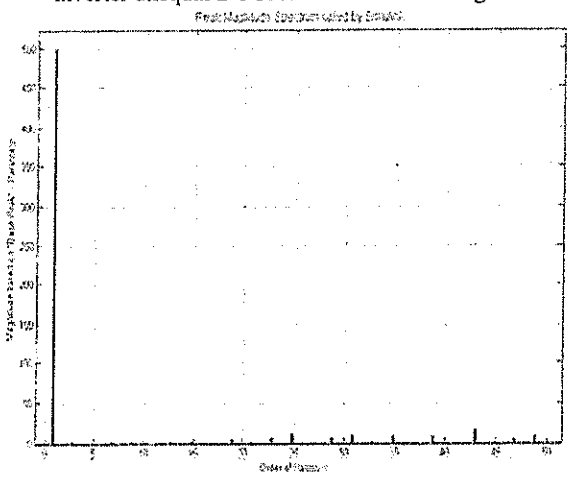

Fig. 17 FFT of the out put voltage for three-phase 11-level unequal DC source inverter at M=0.65 using GA.

With enough levels and an appropriate switching algorithm, the multilevel inverter results in an output voltage that is almost sinusoidal. For the 11-level inverter the waveform has less than 5% THD with each active devices switching only at the fundamental frequency.

8. CONCLUSIONS

An optimization technique based on GA has been used to minimize the THD in multilevel inverters. The GA technique produces possible solutions; the solution which gives the lowest THD is selected. The proposed technique has been applied to an 11-level inverter with equal and unequal DC sources. The proposed inverter configuration has the advantage of its reduction in number of switching devices compared to other configurations of multilevel inverter with same number of levels. It has the drawback of the high rating of the four main switches as they subjected to the summation of DC sources. Simulation results showed that GA is better than previous conventional techniques for minimizing the THD, for different inverter configurations with equal and unequal DC sources.

9. REFERENCES

[1] J. N. Chiasson, L. M. Tolbert, K. J. Mckenzie and Z. Du, "A New Approach to Solving the Harmonic Elimination Equations for Multilevel Converter", 0-7803- 7883-/03/$17.00(c) 2003 IEEE.

[2] J. S. Lai and F.Z. Peng, "Multilevel Converters- a New Breed of Power Converters", IEEE Trans. Ind. Application, Vol. 32, pp. 509-517, May/June 1996.

[3] L. Tolbert, F.Z. Peng, and T. Habetler, "Multilevel Converters for Large Electric Drives", IEEE Trans. Ind. Application, Vol.35, pp 36-44, Jan./Feb.1999.

[4] R. Teodorescu, F. Beaabjerg, J. K. Pedersen, E. Cengelci, S. Sulistijo, B. Woo, and P.Enjeti, "Multilevel Converters- a Survey", in Proc. European Power Electronics Conf. (EPE 99), Lausanne, Switzerland, 1999, CD ROM.,

[5] J. Rodriguez, J. Lai; and F. Zheng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications'', IEEE Trans. Ind. Electronics. Vol. 49, PP 724-738, August 2002.

[6] T. H. Abdelhamid, "Harmonic Elimination of a New Topology Of Multilevel Inverters With Programmed PWM", Journal of Engineering and Applied Science, Vol. 53, No 6, Dec. 2006, PP 785-798, Faculty of Engineering Cairo University.

[7] T. H. Abdelhamid and K. M. Elnaggar, "Optimal PWM Control of A New Generalized Family of Multi Level Inverters", Electric Power Components and Systems, No 36, May-June 2008, pp. 73-92.

[8] N. Celanovic and D. Boroyevic, "A Fast Space Vector Modulation Algorithm for Multilevel Three-Phase Converters", in Conf. Rec. IEEE-IAS Annu. Meeting, Phoenix, AZ, Oct. 1999, pp. 1173–1177.

[9] J. Rodrıguez, P. Correa, and L. Morán, "A Vector Control Technique For Medium Voltage Multilevel Inverters", in Proc. IEEE APEC, Anaheim, CA, Mar. 2001, pp. 173–178.

[10] P. Hammond,"A New Approach To Enhance Power Quality For Medium Voltage Ac Drives", IEEE Trans. Ind. Applicat., Vol. 33, pp. 202-208, Jan./Feb.1997

[11] L. Tolbert and T. G. Habetler, "Novel Multilevel Inverter Carrier-Based PWM Method", IEEE Trans. Ind. Applicat., vol. 35, pp. 1098–1107, Sept./Oct. 1999.

[12] Y. Liang and C. O. Nwankpa, "A New Type Of STATCOM Based on Cascading Voltage-Source Inverters With Phase-Shifted Unipolar SPWM," IEEE Trans. Ind. Applicat., Vol. 35, PP 1118–1123, Sept./Oct. 1999.

[13] L. Li, D. Czarkowski, Y. Liu, and P. Pillay, "Multilevel Selective Harmonic Elimination PWM Technique in Series-Connected Voltage Inverters", in Conf. Rec. IEEE-IAS Annu. Meeting, Oct. 1998, pp. 1454–1461.

[14] S. Sirisukprasert, J. S. Lai, and T. H. Liu, "Optimum Harmonic Reduction With a Wide Range of Modulation Indexes For Multilevel Converters", in Conf. Rec. IEEE-IAS Annu. Meeting, Rome, Italy, Oct. 2000, pp. 2094–2099.

[15] J. Chiasson, L. M. Tolbert, K. McKenzie, Z. Du," Eliminating Harmonics in a Multilevel Converter Using Resultant Theory," Conference Proceedings of IEEE Power Electronics Specialists Conference, Vol. 2, 2002, PP 503–508.

[16] B. Ozpineci, L. M. Tolbert, J. N. Chiassion "Harmonic Optimization of Multilevel Converters Using Genetic Algorithms", IEEE power Electronics Specialists Conference, Aachen, Germany, 2004, PP. 3911-3916.