University: Menoufia

Faculty : Electronic Engineering

Department : Electr. & Elect. Comm.

Academic level: 4th Year

Course Name : Elective Course (5)

Course Code : ECE 416



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Time : 3 Hours

No. of pages : 2

Full Mark : 70 Marks

Exam : Final Exam-Sept Examiners : Dr: Mohamed Salah

د. محمد صلاح طبور --- تصميم الدوائر المتكاملة

Question 1

a) State the Electrical Properties of Digital Integrated Circuits.

(14 Marks)

b) Explain with draw the Seven-stage ring oscillator with a buffered output.

(5)

c) What is meant by $(Fan-In) - (Fan-Out) - (V_T) - (Logic Swing)$?

(2)

d) What is the importance of calculating the noise margins of the logic gates?

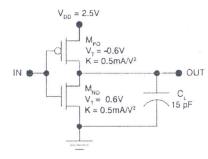
(4)

(6)

Question 2 (14 Marks)

a) Estimate t_P (15-pF load) for the symmetric CMOS inverter depicted in the following figure,

with
$$V_{DD} = 2.5 \text{ V}$$
, $V_T = 0.6 \text{ V}$, and $K = 0.5 \text{ mA/V}^2$.



b) Draw the realization circuit using CMOS and the logic gates level of: Y = (ABC + D) + EF + G

(8)

(6)

(8)

Question 3

(14 Marks)

- a) Lay out a 60-k Ω resistor using a PSELECT layer with a sheet rho of 300 W/square.
- b) Design the layout for a CMOS standard cell that realizes the function Y = ABC + DE.

Question 4

(14 Marks)

a) Realize the following decoder as a distributed gate array.

(7)

A	В	\mathbf{D}_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	0	1	0
1	0	0	0	0	1
1	1	0	1	0	0



b) Draw XOR circuit design as a transistor switch array with: a) depletion implanted overpassb) metal overpass.

Question 5

(14 Marks)

a) Compare between the characteristics of

(6)

- 1- bipolar technology,
- 2- CMOS technology, and
- 3- BICMOS technology.
- b) Draw the circuit diagram of BiCMOS NAND2 gate.

(8)

WITH BEST WISHES

Assoc. Prof. Dr. Mohamed Salah Tabbour