Final Exam

Digital Design

Computer and Syst. Dept.
Time Allowed: 3 hrs.
2nd Year Students.
Dr: Ahmed Saleh
Total Marks: 90
2012 – 2013

Attempt the following questions:

- يسمح باستخدام القلم الرصاص (شرط وضوح الخط).
- الرجاء وضوح الرسم قدر المستطاع (ليس شرطا استخدام المسطرة)
- الامتحان في ورقتين.

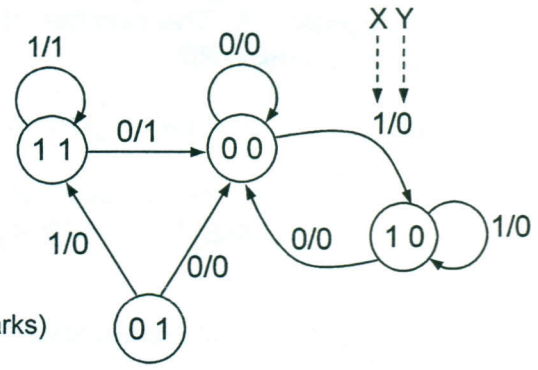
(1) Design the sequential circuit for the state diagram shown in the figure, use J-K flip flops.

(5 marks)

(2) Draw (*ONLY*) the following circuits:

- A ripple counter that counts from 15 to 0 at –ve edge.
- 5-bit shift left register.
- Serial adder circuit.
- 4-bit register with load control.
- A block diagram showing the processor unit.

(10 marks)



(3) Define the following:

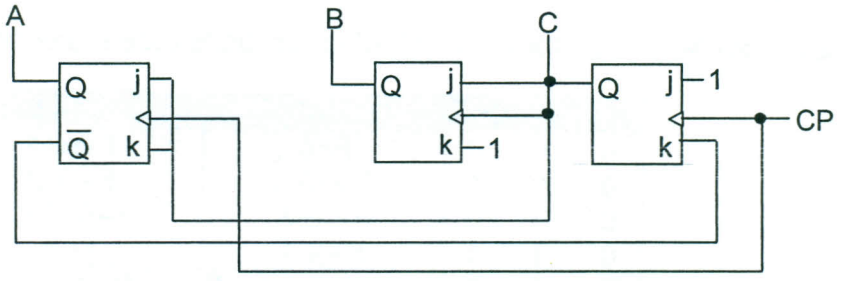
- Flip flop.
- n-bit register.
- n-bit counter.
- Serial and parallel loading (compare in a table). (6 marks)

(4) Design serial subtractor circuit using R-S flip flop. (5 marks)

(5) Design a counter with the following sequence **2, 3, 5, 6, 7, 1, 0, 4, 9** (using T- flip flop).

(5 marks)

(6) For the following 3-bit ripple counter, find the count sequence. Is the counter self starting?



(5 marks)

(7) Design digital system with 3 registers A, B, C and a flip flop E (of J-K type) to perform the following:

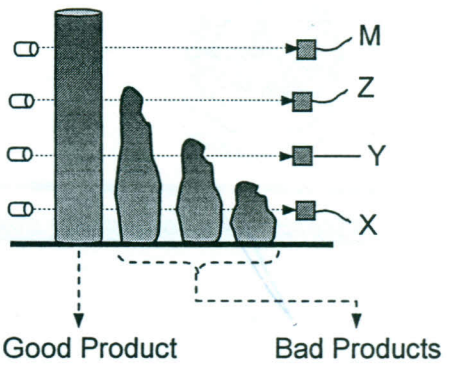
- When a start signal S=1, Transfer two numbers to A and B.
- If A>B: Clear register A and set flip flop E to 1, then increment B in the next clock pulse. Then system stops.
- If A≤B: Clear flip flop E, then,
  - If A<B: shift left A, then add the contents of A (after shift) to B and transfer results to C. Then system stops.
  - If A=B: increment B in the next clock pulse, then system stops.

(10 marks)

اقلب الورقة

(8) Design a digital system to calculate the money that the company will lose due to the bad products as shown in the figure. The system also counts the number of good products (stored in R1), the number of defected (bad) products (stored in R2), and the total number of products (stored in R3). It is noted that; a start signal S initiates the system operation, while a finish signal F terminates the system operation.

(10 marks)



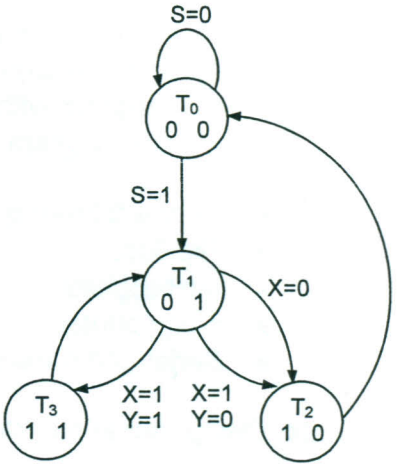
(9) Design a digital system to calculate the number of ones and the number of zeros stored in register RA. The number of ones should be stored in counter R1, while the number of zeros stored in R0.

(10 marks)

(10) Using the state diagram in the following figure:

(a) Find the corresponding ASM chart.
(b) Design the control logic using MUXs.

(6 marks)



(11) Design a universal shift register to perform the following functions:

(8 marks)

S_2	S_1	S_0	Function
0	0	0	Shift Right
0	0	1	Load external input
0	1	0	Clear
0	1	1	Shift left
1	0	0	No change
1	0	1	Load all ones
1	1	0	Clear
1	1	1	

(12) Design an ALU to perform the following functions (use the direct method):

S_2	S_1	S_0	C_{in}=0	C_{in}=1
0	0	0	F=A	F=A+1
0	0	1	F=A-B-1	F=A-B
0	1	0	F=A+B	F=A+B+1
0	1	1	F=A-1	F=A
1	0	0	A ^ B	(AND)
1	0	1	A⊙B	(XNOR)
1	1	0	(A ^ B)'	(NAND)
1	1	1	A'	(NOT)

(10 marks)

---------- End Of Questions ----------

With Best Wishes
Dr: Ahmed Saleh

PLZ, send your comments about the exam to:
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