New Hybrid Superconducting Fault Current Limiter For Primary Distribution Systems

كابح مركب جديد لتيار الخطأ فى نظم التوزيع الابتدائية يعتمد على التوصيلية الفائقة

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ملخص

يقدم البحث تصميما جديدا لكابح لتيار الخطأ فى نظم التوزيع يعتمد على موصل فائق التوصيلية من الجيل الثانى يبرد بالنيتروجين السائل متصل على التوازى مع فرعين أخرين أحدهما معاوقة مكونة من مقاومة و ملف ليتقاسم تيار الخطأ مع الموصل الفائق ويخفض الإجهاد الحرارى عليه و الثانى ثيرستور من نوع GTO مع قنطرة من أربعة ديودات يتم التحكم فيه ليمكن الجهاز من العمل فى أحد نظامين متاحين. فى النظام الأول يقوم الثيرستور بتنظيم حرارة الموصل الفائق و حمايته من الارتفاع المدمر فى درجة الحرارة بينما يمكن الجهاز من العمل بفاعلية بدون الموصل الفائق فى حالة صيانته أو تلفه فى النظام الثانى للتشغيل. ويعرض البحث نظرية عمل الجهاز و طريقة تصميمه والتحكم فيه كما يناقش أداءه أثناء التشغيل فى نظام توزيع بجهد ١١كيلو فولت يحتوى وحدات توليد موزعة و يوضح خواص الأداء والعوامل المؤثرة عليه تحت ظروف خطأ متنوعة كما يقارن مستوى كفاءة الجهاز فى نظامى التشغيل (الأساسى و الاحتياطى).

Abstract

In this paper, a new hybrid fault current limiter is proposed for primary distribution systems. It incorporates a high temperature superconducting element in parallel with other two branches. The first is an inductive impedance to share the fault current with. The second branch is a gate-turn-off thyristor switch controlled to operate the device in either of two modes: the main mode and the stand-by mode. For the main mode, it controls the temperature of the superconducting element and protect it against damaging excessive heating. Instead, in the stand-by mode, it keeps the device applicable without that superconducting element. The design, control and operation of the device is addressed. Its performance in 11 kV distribution systems with DG is investigated. The effect of fault location and fault incidence angle on the device behavior are explored.

1. Introduction

Serious faults can generate current surges of more than 30 times the normal operating current that can be devastating to utility and customer equipment [1]-[5]. A Fault Current Limiter (FCL) is a device placed in electric network to limit the peak fault current. Basically, the FCL is a variable impedance that is installed in series with a circuit breaker. In case of a fault, the impedance rises to a value at which the fault current is correspondingly reduced to a lower level that the circuit breaker can cope with [6]-[12]. The FCL can offer cost-effective means to limit the high level short-circuit currents to lower levels which allow circuit breakers contact to open quickly and safely. Application of the FCL in electric power systems is expected not only to suppress the amplitudes of the short circuit currents but also to enhance the power system stability and quality [1], [13].

It is estimated that by the year 2010, 20-30% of all new installed power generation will be introduced in the form of distributed generation (DG) [1], [13]. DG will contribute largely to fault current in the system resulting in much magnified fault current level. This has an adverse impact on the system switchgear and also on the coordination of the relaying scheme [1]. A remedy is to minimize the contribution of the DG during a fault, while adding no adverse effects to the network

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during normal operation. A candidate solution is to insert a FCL that would limit the current of the DG during a fault, and would otherwise allow the unimpeded flow of power from the DG into the system. This solution does not require any change in the existing relay protection scheme [1], [14].

There is a rapid progress on High Temperature Semiconductors HTS cooled with liquid nitrogen [7], [9]. It is reported that HTS wire based on YBCO-alloy coated conductor provides an optimum tool for development of a practical resistive superconductive fault current limiter (SFCL) [8]-[10]. Due to SFCL's low-loss nature in superconducting state during normal operation, it sets the base for solutions to controlling fault current levels in utility distribution and transmission networks [9], [12]. When the fault current exceeds the critical value of the HTS, superconductivity is lost. Then, SFCL will produce high impedances in the fault current path to limit its value to levels that circuit breakers can manage [8].

During the process of current limiting, the SFCL is at the risk of damage due to overheating. So, a shunt element in parallel with the SFCL device can be added to remove some heat from the superconducting element. Under the normal operation, the SFCL is in superconducting state and short-circuits the shunt element. With the SFCL and the shunt element, the peak value of the limited fault current increases by about 20% that means a decrease in limiting efficiency. This behavior is because the shunt element in parallel with the SFCL lowers obviously the overall limiting resistance of the FCL [12].

To be capable of immediate re-closing after a fault limiting operation as desired, the SFCL temperature must be kept in a superconducting regime. With the HTS material YBCO (YBa2Cu3O7), which has a critical temperature around 90K, this requires keeping the temperature rise below 85K. Unfortunately, this requirement adversely impacts complexity, size and cost [10], [12]. Therefore a more practical target for a SFCL is to provide a single-shot fault limitation with recovery after multiple minutes of cool-down [9], [12]. During these minutes, SFCL must be taken out of the circuit to prevent further heating of the material caused by the restored normal operation current of generally high values in distribution systems [3].

In [11], the design and operation of a solid-state FCL and circuit breaker is presented. It is based on IGBT switches and devoted to low voltage systems of 220V. In [6]-[7], hybrid FCL is analyzed. It consists of three parallel branches: a fast mechanical switch in the first, GTO thyristor in series with a mechanical switch in the second, and a resistor in series with a load switch in the third. The later FCL is used in [1] to limit the fault current level and to maintain relay coordination in distribution systems with DG. Modeling and power system application of SFCL based on HTS element is described in [8]-[10]. The SFCL is employed in [13], [14] to reduce the fault current injected by DG units and to improve the dynamic response of DG.

In this paper, a new hybrid SFCL (HSFCL) is proposed. It incorporates a HTS element in parallel with other two branches. The first is an R-L impedance to share the fault current with the HTS. The second branch is a gate-turn-off (GTO) thyristor switch controlled to work in either of two modes. It controls the temperature of the HTS and protect it against damaging excessive heating in the first mode. Instead, it makes the device usable without the HTS in the second mode. The design, control and operation of the device is addressed. Its performance in 11 kV distribution systems with DG is analyzed. The factors affecting the device efficacy are explored.

2. Theoretical Model of HTS

A basic property of high temperature superconductor is the electric field strength E, which is a function of the current density J, the temperature T and the magnetic flux density B. The magnetic flux density is the sum of the applied field and the self-field due to the current density. If there is no applied field (only self-field), the electric field can be

considered a function of the current density and temperature, $E = E(J,T)$. A homogeneous sample, with a smooth transition from superconducting to normal state, is considered [8], [9]. The most important physical property dominating the current limiting behavior of the SFCL is the E–J characteristic of the HTS and its dependence on temperature T. E–J can be practically subdivided into three sub-regions: superconducting state, flux flow state and normal conducting state [10].

The HTS in its flux flow state usually obeys the so-called power law as [8]:

$$E(J,T) = E_c \left(\frac{J}{J_c} \right)^{n(T)} \quad (1)$$

where both critical electric field E_c and critical current density J_c are functions of temperature. The exponent n is also a function of temperature and can vary in the range $5 < n < 15$.

In normal conducting state [9].

$$E(J,T) = \rho T_c \left(\frac{T}{T_c} \right) J \quad (2)$$

where ρ is the normal resistivity and T_c is the critical temperature of the HTS.

Assuming adiabatic condition, heat dissipated in the HTS will not be transferred to the liquid nitrogen. Thus, no refrigeration is undertaken by the coolant. The expression of the temperature rise versus time is given by

$$C \frac{dT}{dt} = E(J,T).J(T) \quad (3)$$

Integration of this expression leads to the calculation of the temperature rise ΔT reached by the HTS after a certain time. C is the heat capacity per volume.

3.Design of Superconducting FCL

A resistive SFCL limits the fault current by the transition of HTS to increased resistance at fault. The key parameters impacting the resistive SFCL design are the limited fault current (I_{lim}), fault duration (Δt) and permissible temperature rise (ΔT) of the HTS elements [12]. These variables are related by:

$$R = \frac{V_o}{I_{lim}} = \frac{\rho l}{t w} \quad (4)$$

$$I_{lim} = t w \sqrt{\frac{C_p . \Delta T}{\rho \Delta t}} \quad (5)$$

where

R = FCL resistance at fault

V_0 = system rms voltage

l = length of HTS current limiting elements

ΔT = maximum permissible temperature rise

Δt = maximum fault duration (hold time)

ρ, t, w are resistivity, thickness and width of HTS, respectively.

Cp = effective specific heat of HTS and stabilizer.

Therefore, the minimum conductor volume (Vol) for a series FCL is calculated as [12]:

$$Vol = \frac{I_{lim} V_o \Delta t}{C_p . \Delta T} \quad (6)$$

The required minimum conductor volume is noticed to be independent of conductor resistivity.

4. The proposed Hybrid SFCL

Fig.1 shows the structure of HSFCL proposed in this paper. HSFCL has two possible modes of operation which are the normal and the stand-by modes. It is made up of three parallel branches. The middle one is a second generation (2G) YBCO HTS resistive element that constitutes the basic part of the device. Its resistance R is zero at normal operation and ascends non-linearly with time under fault condition due to the effect of temperature rise. A R-L impedance branch Z_{sh} is shunted to the HTS element to share the fault current with the HTS preventing its excessive heating or damage as discussed above.

The value of Z_{sh} influences both the overall limiting resistance introduced by the FCL as well as the fraction of the fault current passing through the HTS. This will define both the fault current limiting capacity of the device and the level of heating in the HTS element. Either a pure resistance or inductor are commonly used in the shunting branch of the HTS element. The R-L impedance is selected instead herein to lower the power losses caused by the mere resistance in one hand and to reduce the voltage oscillations caused by the mere inductor in the other.

Typically, Z_{sh} is chosen to provide enough limiting impedance and to reduce the current flowing through the HTS by about 50% [9], [12]. Therefore, the R_{sh} and L_{sh} elements composing Z_{sh} are chosen as: 9Ω and 20mH, respectively for the system studied in this paper. .

The third parallel branch is a GTO thyristor switch surrounded by four anti-parallel diodes to allow current flow in both half cycles. The GTO thyristor is equipped by a metal-oxide varistor MOV for damping high transient overvoltages protecting the GTO thyristor [7], [11]. For the normal operating mode, the thyristor is normally off and controlled to switch on only after the end of the fault to divert the current from passing through the HTS. So, no additional heating occurs in the HTS by the normal operating current permitting the HTS to cool down and recovers. When the HTS temperature comes back to the superconductivity level, after several minutes of cooling, the thyristor is switched off again. In the stand-by control mode, the HTS branch is assumed open for maintenance or other reasons. The thyristor is controlled to carry the whole circuit current under normal current conditions. If a fault occurs, the thyristor is turned off diverting the fault current to pass through the shunt impedance branch.

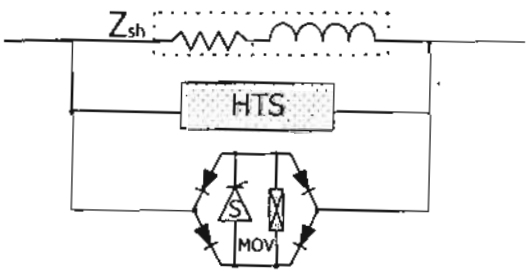

Fig.1 Block diagram of the proposed HSFCL

5.The Control Scheme Of HSFCL

Fig.2 shows the control scheme of the HSFCL. For the normal operation mode, the thyristor switch is controlled to be closed only under either of two conditions. The first is when the fault ends and the HTS temperature exceeds the critical temperature. The second is when the temperature rise of the HTS exceeds the permissible limit due to the excessive heating under fault. The first is for the device functionality and the second for protecting the

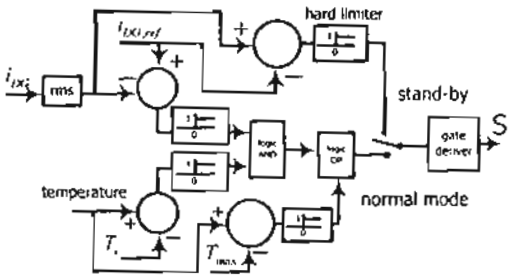

Fig.2 Schematic diagram of the control system

costly HTS. On closing, the thyristor switch will practically short circuit the hot HTS with non-zero positive resistance as well as the shunt impedance. So, the current flows completely in the thyristor leaving the HTS temporarily for some minutes allowing it to cool down to superconductivity temperature. When the HTS comes back to superconductivity level after cooling down, the thyristor is turned off again as the normal state. Thus, the thyristor carries the nominal circuit current for only few minutes following a fault which does not impose any high stresses on. Also, the transition to on and off states occurs under no-fault conditions reducing the transient voltages across the thyristor to moderate levels.

For the stand-by mode, the thyristor is controlled to accomplish the fault limiting task in case of the unavailability of the HTS for maintenance or failure. The thyristor is controlled to be closed under normal operation where it short circuits the shunt impedance and carries the full normal circuit current similar to [11]. When a fault occurs, the thyristor is switched off diverting the current through the shunt impedance Z_{sh} increasing the impedance of the current path. Therefore, the level of the fault current is limited. The thyristor is subjected to much higher stresses with that later mode as it caries the normal circuit current nearly for the whole operation time. Besides, higher transient voltages TRV are expected as the thyristor switches from on to off states under fault.

6. Description of the Study System

Fig. 3 depicts the power system studied in this paper. The performance of the proposed HSFCL in limiting the fault current injected by DG is to be examined. A 6.6 kV 1 MVA three phase synchronous generator is coupled to 6.6/11 kV transformer and integrated to 11 kV 50 Hz three phase ac system through a short overhead transmission line of 20km length. The proposed HSFCL device is connected between the transformer terminals and the near end of the line in each phase. A 1MW, 0.95 lagging power factor three-phase load is supplied at the near end of the line and after the HSFCL. The transmission line is modeled as a distributed parameters line with r=.07 Ω/km, L=1 mH/km and C=1.5x10^{-9} F/km. The synchronous generator is a 6-pole cylindrical rotor machine with a rated angular speed of 104.7 rad/s. The excitation dc current of the generator field circuit is held constant. The generator model is given in [14], [15]. Its electrical torque T_j is calculated by:

$$T_j = \frac{1}{\omega_r}\sum_j \left(V_{L,j} + R_a i_{g,j} + L_a \frac{di_{g,j}}{dt} \right) i_{g,j} \qquad (7)$$

where: j refers to the phases a, b and c, V_L is the DG terminal voltage, R_a is the generator armature resistance (Ω/phase), L_a is the generator armature inductance (H/phase), and i_g is the generator current (A).

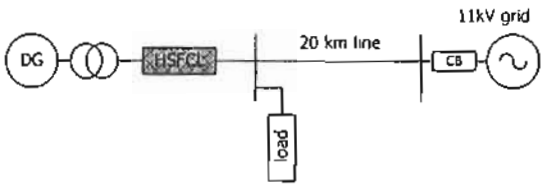

Fig.3 Single line diagram of the study system

7. Performance Results

A full dynamic model of the system depicted in Fig.3 is constructed in the MATLAB/SIMULINK environment. The behavior of the proposed HSFCL is examined under different fault conditions for the two possible modes of operation. The DG current is measured on the 11kV side of the transformer. The performance of the system is analyzed in the following sections.

7.1 Main operation mode

The most severe fault conditions is the three phase to ground fault. So, the performance of the HSFCL is assessed for 3 cases of this fault type at different locations of 5, 1 and 10 km on the distribution line. The selected three locations reflect greatly variant fault current waveform characteristics for the HSFCL. The faults are assumed to start at 0.022 s and ends at 0.122 s.

(a) Fault at 5 km

A symmetrical fault is assumed at 5 km on the line from the DG end. A considerable amount of line impedance will be included in the fault current path. Fig.4a reveals the phase a current of the DG with the HSFCL (the solid) and without the HSFCL (the dotted). Fig.4b shows the three phase currents of the DG. With the HSFCL, the first peak value of the post-fault DG current is about 1500A and is sequentially further reduced in the following peaks. The first peak value of the DG post-fault current is more than 3kA and its steady-state value is higher than 2kA without the HSFCL. This indicates that the HSFCL results in reducing the first peak fault current by about 52%. This factor much increases with the next peaks sequentially to reach about 70% in the last cycle of the fault current. The HSFCL introduces time-increasing resistance in the way of the fault current to restrict its level. It is noted from Fig.4b that the three phase currents have similar variation trends.

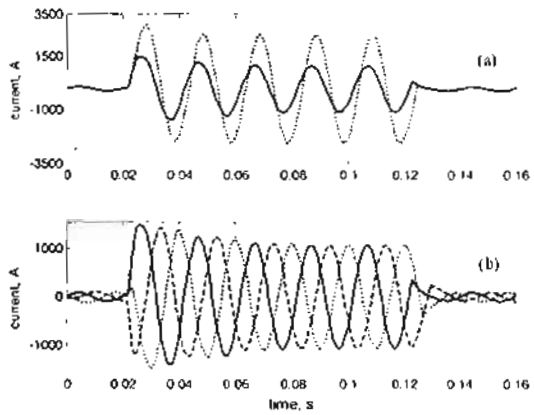

Fig.4 DG current waveforms for fault at 5km

Fig.5a depicts the pattern of resistance change of the HTS wire of the HSFCL against

time for this fault. Fig.5b shows the temperature change of the HTS wire for the same fault.

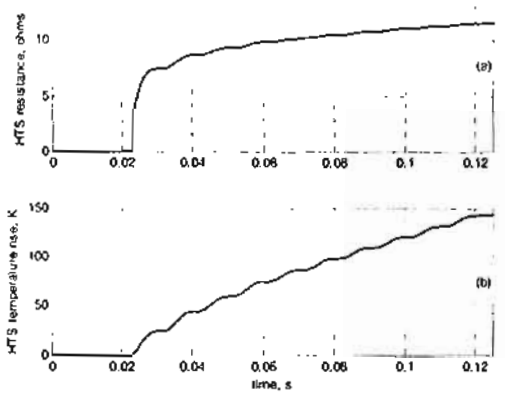

Fig.5 HTS resistance and temperature variation

Fig.6 shows the operation details of the HSFCL. Fig.6a depicts the current distribution in the branches of the device before the thyristor switch is turned on subsequent to the fault clearance. The HTS current is the solid line, the shunt impedance current is the dashed line and the switch current is the dotted. The HTS carries the major part of the DG fault current due to its low resistance at the fault start interval. The HTS resistance increases with time after fault initiation leading to a decrease in current with time. The switch current is zero as it is open during this period. Fig. 6b illustrates the current commutation process in the device branches due to the post-fault switch closing. For this period the control signal of the switch is changed from zero to 1 around 0.014 s as shown in Fig. 6c for the switches in the three phases. At the switching on instant, it is noted from Fig.6b that the HTS current is chopped to zero as the switch bypasses the hot HTS element of about 12 ohms resistance. The shunt impedance current decays nearly to zero after 0.014 s. The normal DG current is almost carried completely by the thyristor switch (the dotted line in Fig.6b).

Fig.7 reveals some performance characteristics of the system. Fig.7a compares the load voltage waveforms for the healthy case (the dotted), the faulty conditions with the existence of the HSFCL (the solid) and the faulty conditions without the HSFCL (the dashed).

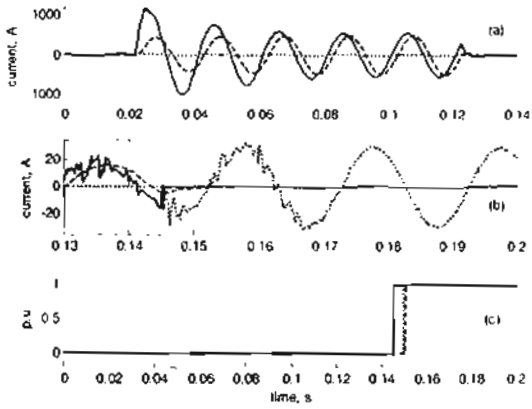

Fig.6 Current distribution in HSFCL branches for fault at 5km

It is remarked that the device greatly improves the load voltage under fault conditions to be very close of the nominal voltage. No deep sag occurs in the voltage which assures high power quality in the system owing to the action of limiting the fault current to much lower levels (Fig. 4a). There is no severe surges in the transient recovery voltage across the device as depicted in Fig.7b. Fig.7c shows the electrical torque of the DG generator with the HSFCL (the solid) and without the HSFCL (the dotted). Without HSFCL, the torque jumps to severe spikes next to the instant of fault start and falls to negative values next to the fault end instant causing the DG to work as a motor which is unwanted. This situation vanishes when the HSFCL is included and the dynamic response of the machine in clearly improved in agreement with [13], [14].

(b) Fault at 1 km

A symmetrical fault is assumed on the line at 1 km from the DG end. A minor amount of line impedance will be included in the fault current path. Fig.8a reveals the phase-a current of the DG with the HSFCL (the solid) and without the HSFCL (the dotted). Fig.8b shows the three phase currents of the DG. With the HSFCL, the first peak value of the post-fault DG current is about 1500A and is further reduced sequentially in the following peaks. Without the HSFCL, the first peak

value of the DG post-fault current is more than 6kA and its steady-state value is higher than 5kA. This indicates that the HSFCL results in reducing the first peak fault current by about 68%. This factor much increases with the next peaks to reach about 83% in the last cycle of the fault current.

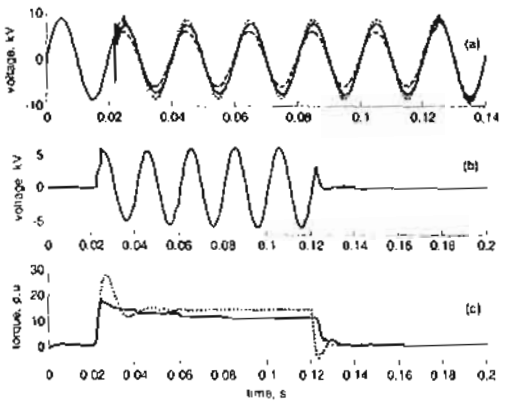

Fig.7 Voltage and torque signals for fault at 5km

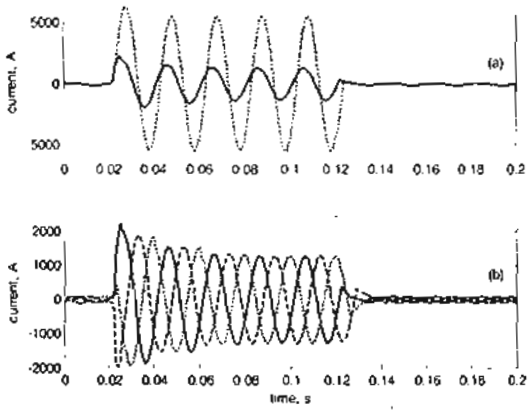

Fig.8 DG current waveforms for fault at 1km

(c) Fault at 10 km

A symmetrical fault is assumed on the line at 10 km from the DG end. A large amount of line impedance will be included in the fault current path. Fig.9a reveals the phase-a current of the DG with the HSFCL (the solid) and without the HSFCL (the dotted). Fig.9b shows the three phase currents of the DG. With the HSFCL, the first peak value of the post-fault DG current is about 1.1 kA and is further reduced in succession for the following peaks. Without the HSFCL, the first peak value of the DG post-fault current is more than 1.8 kA and its steady-state value is higher than 1.5kA. This indicates that the HSFCL results in reducing the first peak fault current by about 39%. This factor much increases with the next peaks to reach about 45 % in the last cycle of the fault current.

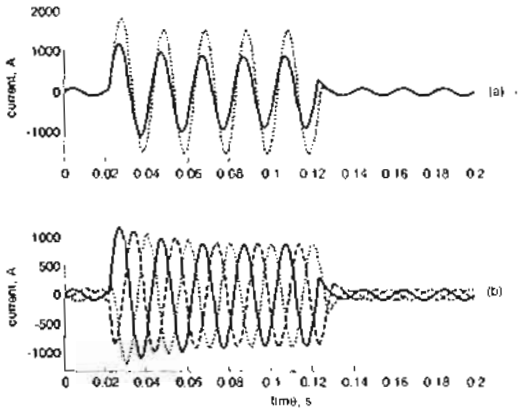

Fig.9 DG current waveforms for fault at 10km

7.2 The stand-by mode

In the stand-by mode, the device has only two branches as the HTS is being removed. The thyristor switch is normally closed for no fault condition. The control scheme is set on the stand-by mode. A symmetrical fault is assumed at 5 km on the line from the DG end. A considerable amount of line impedance will be included in the fault current path. Fig.10a reveals the phase-a current of the DG with the HSFCL (the solid) and without the HSFCL (the dotted). Fig.10b shows the three phase currents of the DG. With the HSFCL, the first peak value of the post-fault DG current is about 2 kA and is further reduced in the following peaks. Without the HSFCL, the first peak value of the DG post-fault current is more than 3kA and its steady-state value is higher than 2kA. This indicates that the HSFCL results in reducing the first peak fault current by about 33% that is less than its peer in the normal mode. This factor much increases with the next peaks to reach about 75%.

Fig.11 is analogous to Fig.6. Fig.11a shows that the inductive impedance branch carries the whole DG fault current as the thyristor switch opens on sensing a fault.

Fig.11b illustrates the current commutation process in the device branches due to the post-fault switch closing. For this period the control signal of the switch is changed again from zero to 1 around 0.015 s as shown in Fig.11c for the switches in each phase. At the switching on instant, it is noted from Fig.11b that the inductive impedance current decays to zero as the turned-on thyristor bypasses it. The whole normal DG current is diverted to the thyristor.

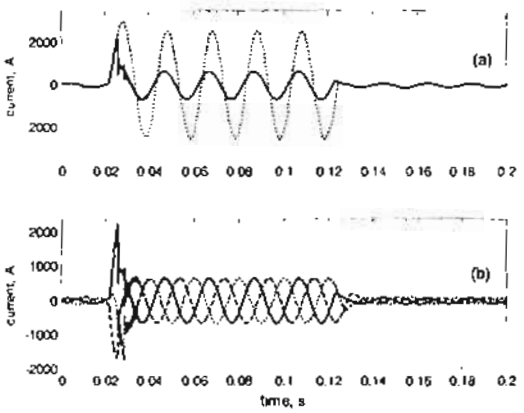

Fig.10 DG current waveforms for stand-by mode

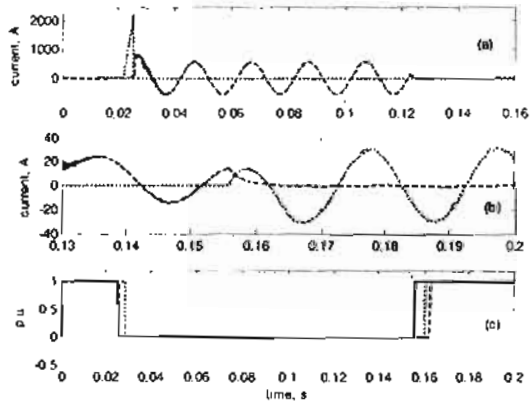

Fig.11 Current distribution in HSFCL branches for stand-by mode

Fig.12 is equivalent to Fig.7. Fig.12a clarifies that the device greatly improves the load voltage under fault conditions to be very close of the nominal voltage. There is some oscillatory transients and spikes for nearly half a cycle after the instant of fault occurrence in the transient recovery voltage across the device as depicted in Fig.12b. The spikes level reaches about 35 kV and is controlled by the MOV across the thyristor. This arises due to sudden diversion of the high fault current to the inductive impedance branch on fault initiation. The oscillations are clearly damped if a resistor replaces the inductive impedance that is recommended for this mode of operation to avoid high voltage spikes (see Fig.13). Without HSFCL, see Fig.12c, the torque jumps to severe values next to the instant of fault start and falls to negative values next to the fault end instant causing the DG to work as a motor which is unwanted. This problem is overcome when the HSFCL is included. Fig. 13 is the equivalent of Fig.12 but when the R-L impedance is replaced with a resistance of the same value in Ω.

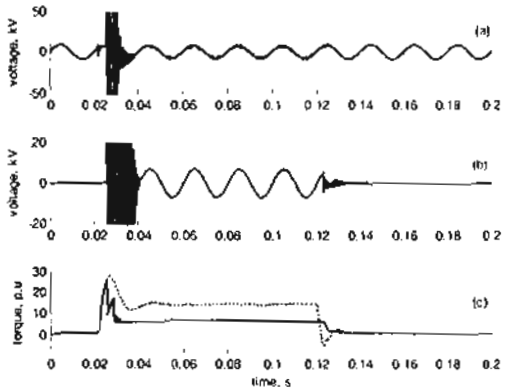

Fig.12 Voltage and torque signals for stand-by mode with the impedance Z_{sh}

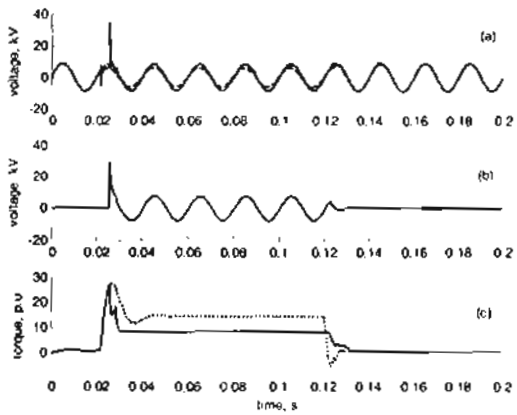

Fig.13 Voltage and torque signals for stand-by mode with a resistance

7.3 Parameters effect

Table 1 compares the DG peak fault current and peak torque with a without the HSFCL at

different fault locations. The fault conditions are the same as in section 7.1. The last row of this table corresponds to the case described in section 7.2. Fig.14 depicts the effect of fault location on the HSFCL-caused percentage reduction in the first peak DG current, the fifth peak DG current (the last faulty peak) and the DG electrical torque. It is worthy to note that the role of the device is more tangible for the faults near to the DG where higher fault currents are anticipated from the DG side. Table 2 shows the effect of fault inception angle (the fault initiation instant) on the performance of the HSFCL. The angle zero is for a fault starting at .02 s. The fault is assumed to a symmetrical three phase fault on the transmission line at 5 km from the DG end with the device on the main mode. The fault angle effect is noticed to be slight for most performance indicators. For example, it causes a variation to the HTS temperature rise in the range of 7K.

Table 1 Effect of fault location on HSFCL performance

Fault location km	With HSFCL		Without HSFCL	
	I_{DG} first peak (kA)	Peak T_{DG} (p.u)	I_{DG} first peak (kA)	Peak T_{DG} (p.u)
0	2.6	34	8.2	80
1	2.1	27	6.4	60
5	1.5	18	3.1	28
10	1.15	13	1.8	18
15	0.96	10.7	1.33	13.6
20	0.8	9	1.04	10.5
5@ stand-by	2	23	2.65	28

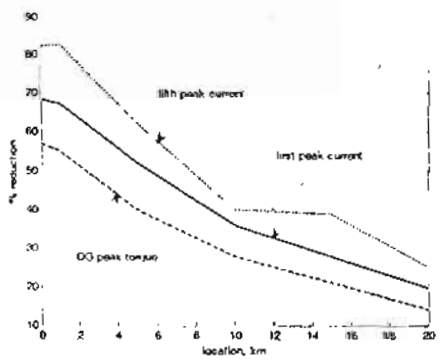

Fig. 14 Effect of fault location

Table 2 Effect of fault inception angle

Fault inception angle (degrees)	With HSFCL			Without HSFCL	
	I_{DG} first peak (kA)	Peak T_{DG} (p.u)	ΔT	I_{DG} first peak (kA)	Peak T_{DG} (p.u)
0	1.5	18	147	3.1	28
36	1.5	18	148	3.1	28
72	1.52	19	144	3.1	28
108	1.53	19	147	3.1	29
144	1.53	19	145	3.06	29
180	1.52	19	152	3.13	29
216	1.53	19	151	3.07	29

8. Conclusion

A new hybrid superconducting FCL is proposed in this paper. It incorporates a HTS element in parallel with other two branches. The first is an inductive impedance to share the fault current with the HTS. The second branch is a GTO thyristor switch controlled to work in either of two modes. It controls the temperature of the HTS and protect it against damaging excessive heating in the main mode. However, it keeps the device usable without the HTS in the stand-by mode. The design, control and operation of the device is presented. Its performance in 11 kV distribution systems with DG is analyzed. The device is proved to be lucidly efficient in limiting the peak fault current of DG units for its two modes of operation. The first mode performance is superior to the second mode from both the limiting efficiency and the transient voltage oscillations. The degree of reduction is generally above 30% and depends on the fault location with respect to the device. It also improves the dynamic response and stability of DG.

9. References

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