Mansoura University		Second Semester - Final Exam.
Faculty of Engineering		Exam Time: 3 Hours
Department of Electronics and Communications Engineering		Subject: Microprocessors Course code: COM 9323
3rd Year Electronics & Comm.	Open Book Exam	Exam Date: 2-6-2014

Attempt all questions. Assume any missed data. Full Mark is 100

Q.1) Correct the errors, if any, in the following statements: [20 Marks]

a. $(1101101.101)_2$ is equivalent to $(109.125)_{10}$.
b. Transistors are reliable and faster than core memory for performing computations.
c. The 4004 used transistors with a feature size of 1000 nanometers.
d. When power save is required, low threshold voltage devices are used.
e. Improvements in interconnect capacitance are possible through further reductions in the permittivity of inter-level dielectrics.
f. The assembler is a program written to convert assembly instructions into its corresponding M/C code.
g. In interrupt-driven I/O, interrupts are used to initiate and/or terminate data transfers.
h. Protected mode is the native state of the processor that provides the highest performance.
i. Scaled-index addressing uses 8 bit registers.
j. The intra-segment jump is a jump anywhere within the current code segment.
k. The stack memory is LIFO.
l. EEPROM is faster than flash memory.
m. A usage bit could be added to indicate whether the page has been changed.
n. Cache is accessed by address.
o. If the clock is operated at 4 MHz, one 8086/8088 bus cycle is completed in 80 μs.
p. In 8086, minimum mode is obtained by connecting the mode selection pin to 5V.
q. The 80188 contains 8-bit data bus.
r. The PCB is a set of 128 registers located in the I/O or memory space.
s. The Pentium pro is packaged on a Printed Circuit Board (PCB) instead of the integrated circuits of the past Intel microprocessors.
t. Intel Core Duo technology is based on two enhanced Pentium M cores that were integrated and use a shared L1 cache.

Q.2) Complete the following statements: [20 Marks]

a. To execute a program stored in main memory, the CPU controller performs .....
b. All commercial computers are based on..... concept, with programs and data sharing the same main memory.
c. ..... supports 8, 16, and 32-bit transfers between the personal computer and memory or I/O at rates of 8 MHz.
d. Memory can be accessed using any of three memory models; ....., ..., or .....

e. The ..... register contains the offset in the current code segment for the next instruction to be executed.

f. ..... applies to a MOV between a memory location and AL, AX, or EAX.

g. Program memory addressing modes used with the JMP instruction consist of three forms; ....., ..., and .....

h. Erasing an ..... requires a special tool that emits ultraviolet light.

i. ..... is the time required to access the requested information in a given level of memory.

j. In ..... locality, accesses tend to be clustered in the address space.

k. ..... updates both the cache and the main memory simultaneously on every write.

l. ..... is an imaginary memory location in which all addressing issues are handled by the operating system.

m. The Fully Buffered 8088 requires ....., ..., and .....

n. In 80186, the interrupt controller operates in two modes; ..... or .....

o. ..... is a special way of handling memory accesses so the memory has additional time to access data.

p. The ..... defines information about the system's tables, tasks, and gates.

Q.3) Choose the most suitable answer in each of the following: **[5 Marks]**

1. The ..... pin is used to insert wait states into the timing of the 8086 microprocessor.

   a) READY c) INTR

   b) NMI d) CLK

2. In 80186, the .... pin informs the µP that the memory is ready for read/write

   a) RD c) SRDY

   b) ARDY d) WR

3. In 80386, the ..... pin is driven by a clock signal that is twice the operating frequency of the 80386.

   a) BS32 c) CLK2

   b) BUSY d) BREQ

4. In 80486, the ..... pin provides a memory system like the 1 MB real memory system in 8086.

   a) A20 c) A2

   b) ADS d) A20M

5. In Pentium, the ..... pin provides even parity for the memory address.

   a) APCHK c) BCHK

   b) BUSCHK d) AP

6. In Pentium, the ..... pin shows that the inquire cycle found a modified cache line.

   a) HIT c) KEN

   b) HITM d) FLUSH

7. In 80486, the ..... pin causes the µP to access byte-wide memory components.

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a) BOFF
c) BS16
b) BS8
d) BREQ

8. The ..... pin = 0 when the temperature of the Pentium II exceeds 130° C.
   a) POWERGOOD
   c) THIRMTRIP
   b) TESTHI
   d) STPCLK

9. The ..... pin i/p causes the Pentium Pro to enter SMM of operation.
   a) SMI
   c) SMMEM
   b) EMI
   d) SMIACT

10. The ..... pin must be connected to +2.5V through a 1K-10K resistor for proper Pentium II operation.
   a) TCK
   c) TDI
   b) TESTHI
   d) TDO

Q.4) Give a *short answer* to each of the following questions: **[9x3=27 Marks]**

a. *"In 2000, some semiconductor manufacturers switched from using aluminum wires, to copper wires"*. Give reasons and state why copper was not used previously.

b. Compare between *write-back* and *write-through* as cache writing policies.

c. Compare between paging and segmentation. Do you think that paging combined with segmentation can introduce better performance? Justify your answer.

d. Define "*fan-out*". What modifications must be done to attach more than 10 unit loads to any bus pin in a 8086 microprocessor?

e. *"The 80486 microprocessor has many improvements than the 80386"*. Compare between the 80386 and the 80486 microprocessors.

f. *"The Pentium III may suffer from serious problems if bus speed increases to 200 MHz"*. What problems would you expect? How to overcome these problems?

g. Can "*Windows XP*" be considered as a real-time operating system 'RTOS'? Why? Suggest other operating systems you think they approach the concept of RTOS.

h. *Using neat sketches*, compare between the non-pipelined and the pipelined read timing for the 80386 µP. Comment on results.

i. *"In order to meet the performance and power targets when designing a dual core processor, Intel had to take some factors into considerations"*. List these factors and comment on them, if you can.

Q.5.a) Implement the following instructions (*Assume EAX=100, BX=1000, SI=10, DS=100*)

a. MOV CL, 100
b. MOV DI, [EAX+100H]
c. MOV DX,[BX+SI+10H] **[6 Marks]**

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e. The ..... register contains the offset in the current code segment for the next instruction to be executed.

f. ..... applies to a MOV between a memory location and AL, AX, or EAX.

g. Program memory addressing modes used with the JMP instruction consist of three forms; ....., ..., and .....

h. Erasing an ..... requires a special tool that emits ultraviolet light.

i. ..... is the time required to access the requested information in a given level of memory.

j. In ..... locality, accesses tend to be clustered in the address space.

k. ..... updates both the cache and the main memory simultaneously on every write.

l. ..... is an imaginary memory location in which all addressing issues are handled by the operating system.

m. The Fully Buffered 8088 requires ....., ..., and .....

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o. ..... is a special way of handling memory accesses so the memory has additional time to access data.

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Q.5.b) Suppose that cache access time is *10 ns*, main memory access time is *90 ns*, and the cache hit rate is *99.2%*. Find the effective access time. If paging is used and the page fault rate is *1%* and it costs us *8 ms* to access a page not in memory, find the effective access time. Comment on results. **[6 Marks]**

Q.5.c) Suppose that we have a virtual address space of 2^{15} words for a given process and physical memory of 2^{13} words. Assume also that pages are 2^{10} words in length. Find:

- The number of bits in virtual address
- The number of bits in physical address
- The number of pages in virtual memory
- The number of frames in physical memory
- The number of bits in page field and offset field
- Suppose the system now generates the virtual address14 , page 0 in virtual memory maps into page 4 of physical memory, find the corresponding physical address both in binary and decimal forms. **[8 Marks]**

Q.5.d) Suppose a computer using set associative cache has 2^{16} words of main memory and a cache of 32 blocks, and each cache block contains 8 words.

- If this cache is 2-way set associative, what is the format of a memory address as seen by the cache?
- If this cache is 4-way set associative, what is the format of a memory address as seen by the cache? **[5 Marks]**

Q.5.e) Write an assembly code to perform the same operations of the following BASIC code :

```
For i=0 to 2
        For j=0 to 3
                Array1( i*4 +j )= i + j
        Next j
Next i
```

[5 Marks]

Hints:

1. Define Array1 as byte variable and compute its length from the basic program and initialize it with any valid data
2. The indices of the outer loop and of the inner loop will be ECX, so you have to save the ECX value of the outer loop before starting the inner loop.

My best wishes to all of you!!

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