equipment for test application and measurement makes functional testing very expensive.

A pseudo random testing approach for mixed-signal circuits is proposed [5]-[6]. In this technique, linear time invariant (LTI) analog circuits are assumed. Many analog blocks in a mixed-signal circuits posses the LTI property and can be efficiently tested using this approach.

A set of signatures for classifications is used instead of the directly measured performance parameters. Thus, the satisfaction and violation of the performance parameters were implied by the signature set. This is called implicit function testing.

The pseudo-random testing approach can constitute an integrated environment for testing mixed-signal circuits. The pseudo-random testing technique requires modeling the analog part as a digital system by embedding the analog part between a DAC and ADC, applying digital pseudo-random test patterns to the modeled digital system, and constructing the signatures based on the cross correlation between the input and output responses.

The basic interesting feature of random testing is its simplicity of implementation and development. There is no need for fault hypothesis to generate random sequences.

The main weakness of random testing is the length required reaching high defect coverage.

The discrete system using an input output interface card, an electronic scanner card and the previous testing methodology were already implemented. The random test sequences (LFSR) and the MISR were realized in the controller in a software manner [7].

Over the last decade, the integrated design technology has become a major and leading-edge global area of high technology offering a wide range of products to facilitate the accelerating change in the power of microprocessor –based products and system.

New trends in electronic circuits are to be small size, low cost, high speed, and low power consumption [8].

Low power design is becoming a new era in VLSI technology, as it impacts many applications using battery-powered portable systems such as notebook, cordless and cellular telephones, etc.

In this paper we will present a realized complete automatic testing equipment using random testing approach on one chip using a low power low voltage FPGA 400K XCV 400 pg560 chip.

Field Programmable Gate Array (FPGA)

A Field Programmable Gate Array (FPGA) is a large Programmable Logic Device (PLD) that can be used to implement large logic equations, as well as arbitrary combinationl and sequential logic circuits. Thus, an FPGA can also be used

to implement the control-logic design. However, we have to keep in mind that an FPGA is a single chip. FPGAs have a much more flexible architecture based on the logic block concept. A logic block consists of a small number of logic. Each FPGA consists of a large number of these logic blocks. Each logic block is connected to another logic block and I/O pins as required, by programmable routing. This enables the inputs to the logic blocks to be connected to input pins or the outputs of other logic blocks, and the outputs to output pins or to input of further logic blocks.

System Configuration:

A low power low voltage FPGA 400K XCV 400 pg560 chip was used for the system under study. Figure (1) shows the total system configuration, which consists of a controller, FPGA system chip, an analog to digital interface unit, and the board under test. The system controller is used to control data transfer, contains the system database. FPGA system chip contains LFSR, MISR, MUX, and input/output ISA compatible interface unit. The analog to digital interface, which consists of an A/D and D/A, circuits for hybrid boards applications. The board under test consists of hybrid circuits, which was used to test the implemented system.

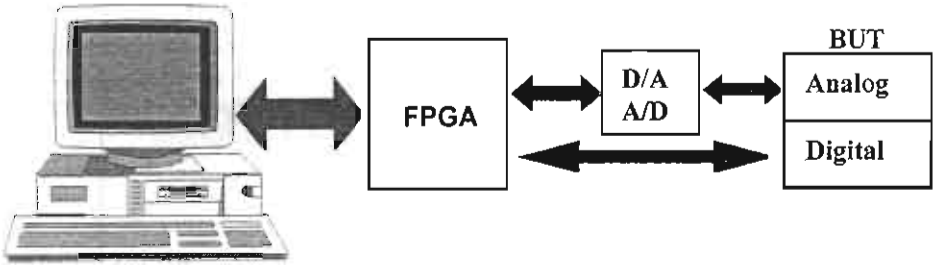

Fig. (1) System block diagram

FPGA Chip Configuration:

Fig (2) shows the complete chip configuration, which represents the hardware design and also the data flow. Two LFSR were designed to generate the random pattern for analog and digital modules, due to speed difference between analog and digital responses. A multiplexer was designed to select between the two LFSR generators according to requirements (MUX_pn). The computer clock coupled with a counter to decrease its rate was used for the system. Digital data coming from board under test is entered through an MISR, which was designed, on the chip for digital testing signature. Two extra modules were designed and coupled to the MISR for signature extraction due to required number of data sequences (S_Register and Data_R). For input/ouput interface two modules were designed with ISA compatible interface (PPI, and a decoder {AD_bus}). To overcome the problem of analog signature instability analog data entering the system is totally stored. To select between data entering the chip (either digital or analog) a multiplexer was designed at data entry pins (MUX_in). The Mentor Graphics Tools for FPGA design were used in this work. The truth table design technique was used for the design of the MUX and the decoder. VHDL was used to design LFSR, MISR , counter, S_register, Data_R, and PPI.

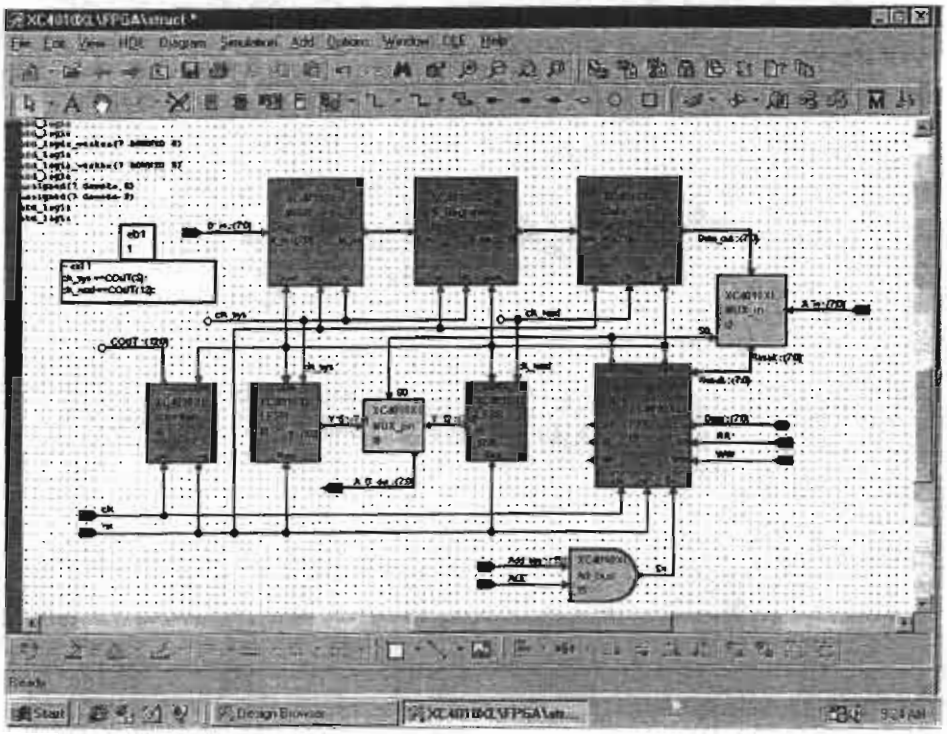

Fig. (2) Chip Configuration

The VHDL entity declaration for PPI is shown below.

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
ENTITY IO_PPI IS
  PORT(
    En    : IN    std_logic ;
    rst   : IN    std_logic ;
    clk   : IN    std_logic ;
    ww    : IN    std_logic ;
    rr : IN    std_logic ;
    Result : IN std_logic_vector (7 DOWNTO 0);
    S0    : OUT   std_logic ;
    S1    : OUT   std_logic ;
    Start   : OUT   std_logic ;
    R   : OUT   std_logic ;
    W   : OUT   std_logic ;
    Data  : INOUT std_logic_vector (7 DOWNTO 0)
  );
END IO_PPI ;
```

Results:

In order to test our designed system a testing configuration was used using hybrid BUT. Figure (3) shows the testing configuration which consists of the system FPGA chip designed BUT and an address checker. Digital part was designed using Mentor Tools and the analog responses were simulated. Digital designed BUT block diagram is given in figure (4). Fig (5) illustrate program output screen for no error condition for the board under test. Fig (5) shows a sample of the input sequence to the BUT from the LFSR generated from the designed system. It also gives the final output signature from the MISR after 128 input sequences. Similarly fig. (6) shows a sample of the input sequence to the BUT from the LFSR generated from the designed systemand the final output signature from the MISR after 128 input sequences for given error (output z shown in fig (4) stack at zero).

Table (1) gives a summary of signatures for different single errors condition in the BUT. The table shows that error recognition is 100%, where signatures are completely different for each error. Figure (7) shows the chip layout for the designed system chip.

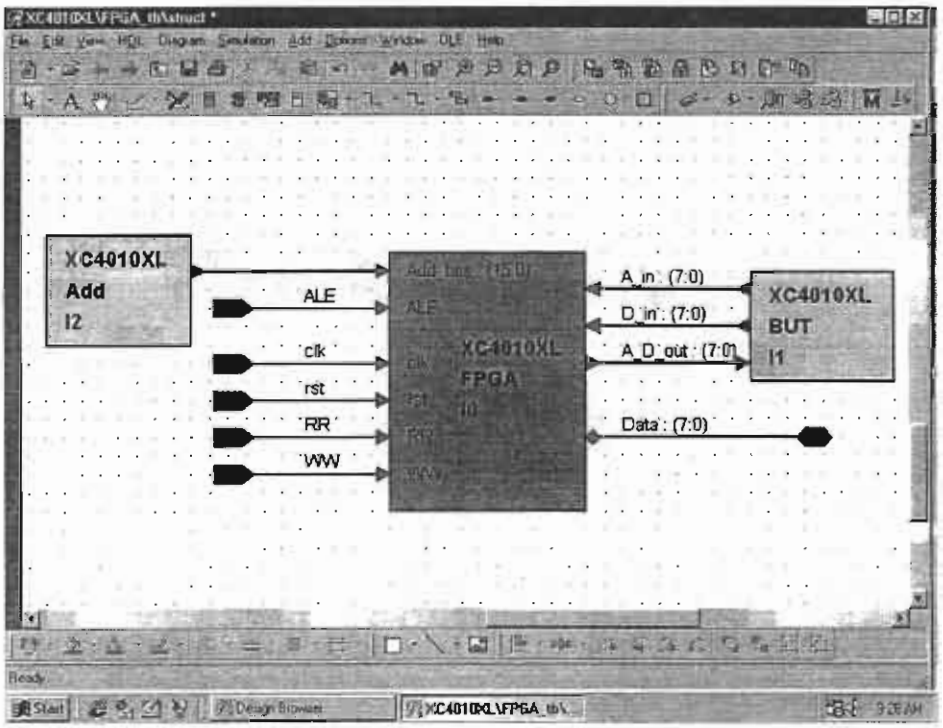

Fig. (3) Testing Configuration

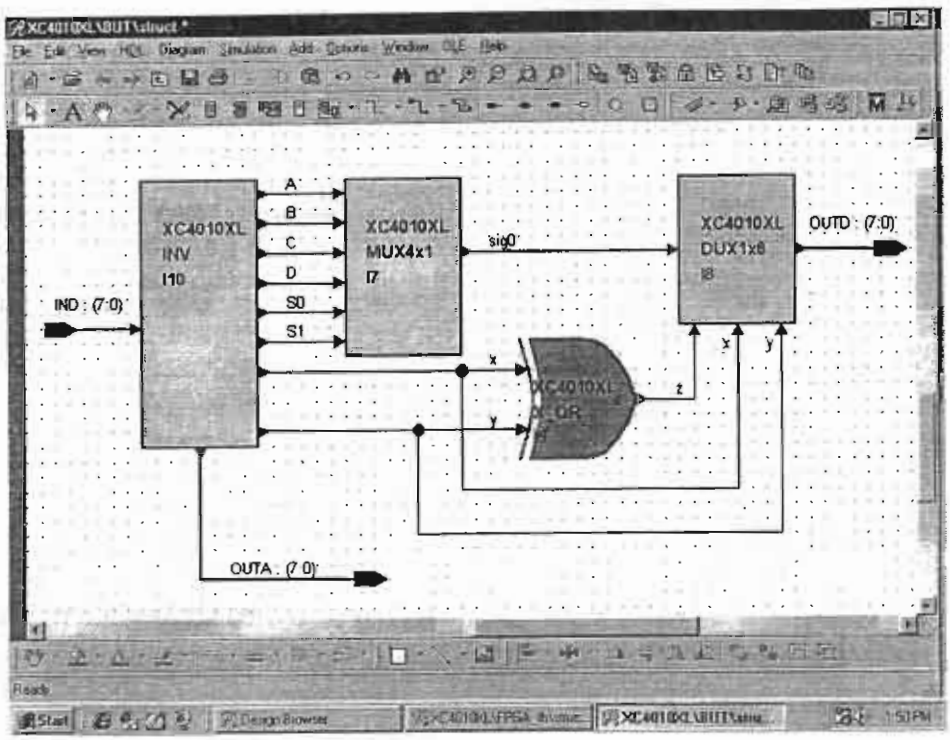

Fig (4) BUT block diagram

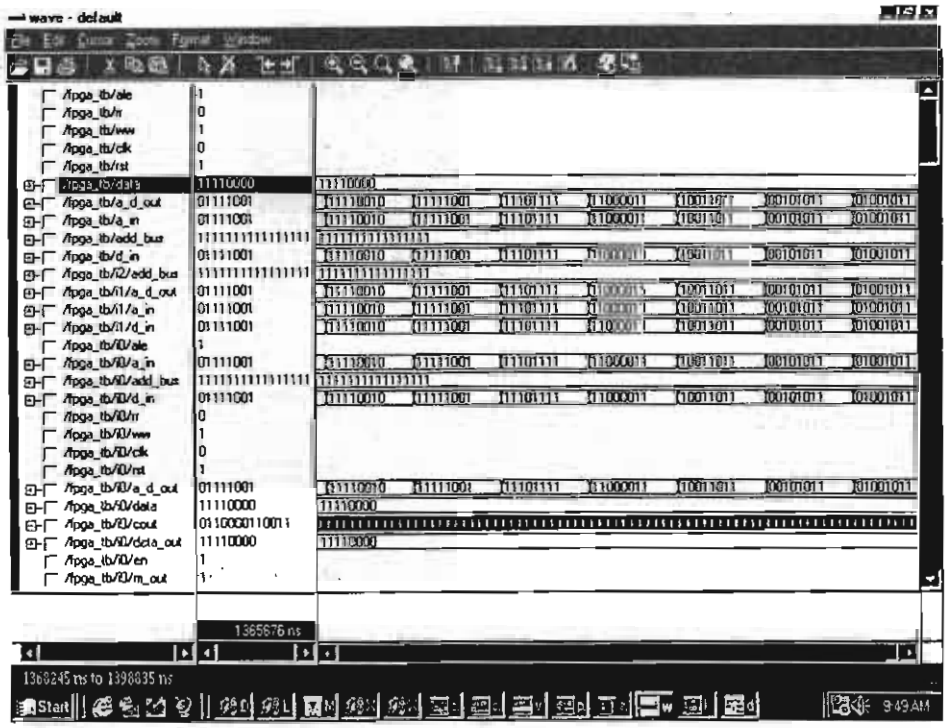

Fig (5) No Error Signature

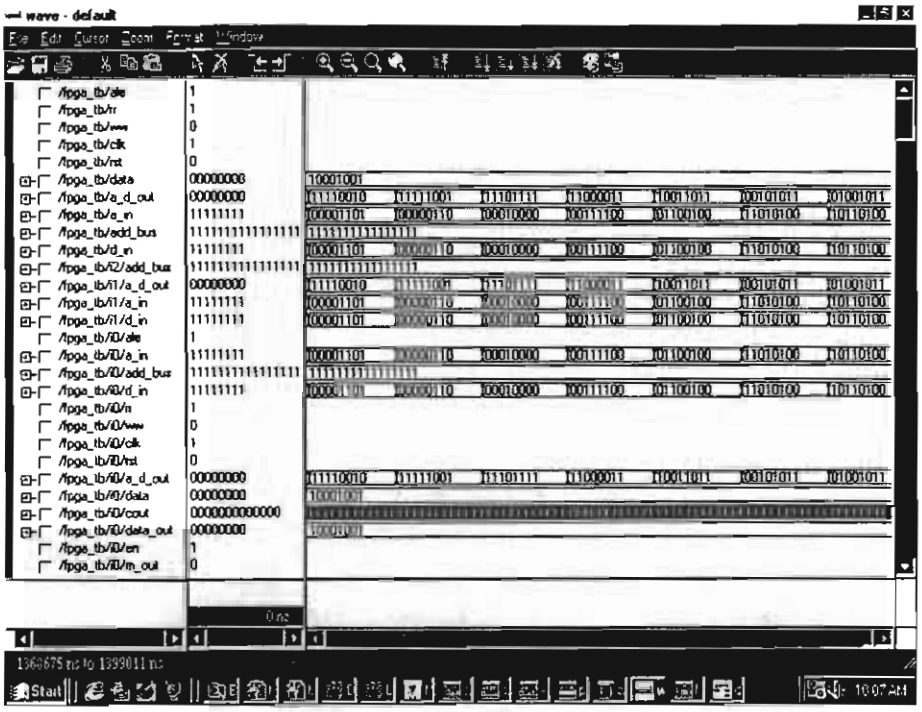

Fig (6) Error signature

Table (1) show some of other error

Error	Signature	Error	Signature
A Stack at o	10010101	A Stack at 1	11001111
B Stack at o	11100010	B Stack at 1	01011101
C Stack at o	01001100	C Stack at 1	00000011
D Stack at o	11001011	D Stack at 1	10010010
S0 Stack at o	10100111	S0 Stack at 1	00011011
S1 Stack at o	10000101	S1 Stack at 1	10100000
X Stack at o	01111100	X Stack at 1	11010001
Y Stack at o	11001001	Y Stack at 1	11010111
Z Stack at o	10001001	Z Stack at 1	11111111
Sig0 Stack at o	00000000	Sig0 Stack at 1	11110011

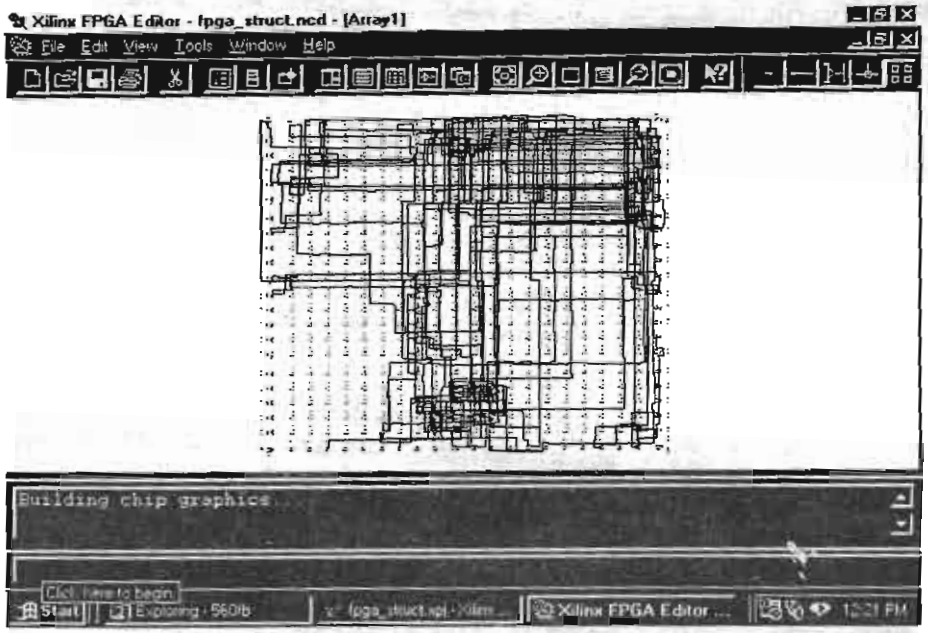

Fig (8) Chip layout

Conclusion

In this paper one chip hybrid automatic testing system was designed, implemented and tested. A low power low voltage FPGA 400K XCV 400 pg560 chip was used in the implementation and design procedure. The testing methodology is based on pseudo random testing strategy. The implemented ATE chip system can be simply used to test automatically any type of hybrid boards The implemented ATE chip system was tested for single error condition and had shown a high error coverage.

List of abrivations

FPGA : Field Programable Gate Array
ATE : Automatic Testing Equpment
LP/LV: Low Power Low Voltage
MISR : Multible Input Sift Register
LFSR : Linear Feedback Shift Register
LTI :linear time invariant
PLD : Programmable Logic Device

References:

1. K.Baker, A.M.Richardson, A.P.Dorey, "Mixed Signal Test Techniques, Applications and Demands", IEE Proc. Circuits, Devices, and Systems, Vol.143, No.6 December 1996
2. L.S.Milor, "A Tutorial Introduction to Research on Analog and Mixed Signal Circuits", IEEE Trans. CAS, Vol.42, No.10, OCT. 1998 pp.1389-1407
3. J.Rajski, J.Tyszer, "Testing of Telecommunication Hardware", IEEE Comm. Magazine, pp.60-62, June 99
4. Stanley Hurst, "VLSI Testing, Digital and Mixed Analogue/Digital Techniques", published by the Institute of Electrical Engineers, London, United Kingdom, 1998
5. C.Y.Pan, and K.T.Cheng, "Pseudo-random Testing for Mixed Signal Cireuits", IEEE Trans. CAD, Vol.16, No.1, Oct. 1997, pp.1175-1185
6. R.David, "Random Testing of Digital Circuits: Theory and Applications", Marcel Dekker, 1998

7.EL.M.Saad, A.E.Salama, H.H.Aamer, I.S.Ashour, M.Hanna, S.El Tawel, K.Abdel Hammed,I.El Said, "Automatic Testing Equipment For Hybrid Boars Using Pseudo Random Testing Approach, Al-Azhar University Engineering Journal,Volume 4, No 3, July 2001,Cairo, Egypt.

8.Anantha P. Chandrakasan, Samuel Sheng, Robert W. Brodersen, "Low Power CMOS Digital Design", EECS Departement, University of California at Berkeley