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MODELING AND ANALYSIS OF MULTI-LEVEL INVERTERS FOR POWER QUALITY PURPOSES

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ABSTRACT
Multilevel inverter technology has become the most appropriate utilization for high-power medium-voltage drives and transmissions. This paper includes a comparative analysis of the performance of 3-level and 5-level inverters connected to induction motor for power quality purposes. It's likely to show the benefits of increasing the number of levels in an inverter. A simple space vector modulation algorithm is used for this comparison. This algorithm is applied to Cascaded Multilevel inverter topology. Power quality of these schemes can be enhanced by eliminating the noisy harmonics. In order to reduce the total harmonic distortion of the resulted voltage waveform a passive filter is carefully designed. In this paper, simulation results are carried out using Matlab/Simulink software environment.

لقد أصبحت تقنية عواكس الجهد متعددة المستويات الاستخدام الأمثل للمحركات وخطوط النقل ذوي القدرات الكبيرة والجهود المتوسطة. تشمل هذه المقالة تحليلاً مقارناً لأداء العواكس ذوي المستويات الثلاث والخمس متصلين بمحرك حثي لأغراض جودة القدرة. من المتوقع ظهور فوائد زيادة المستويات لأي عاكس. لهذه المقارنة، تم استخدام خوارزمية سهلة لتشكيل متجهات الفراغ. هذه الخوارزمية تُطبق على عواكس الجهد من النوع المتتالي. ومن الممكن تحسين جودة القدرة لهذه النظم بازالة التوافقيات المزعجة. تم تصميم مرشح خامل بعناية من أجل تقليل تشوه التوافقيات الكلي المصاحب لموجة الجهد الناتجة. في هذه المقالة، نتائج المحاكاة تم استخراجها باستخدام نظام المحاكاة الماتلاب.

Keywords: *Multilevel inverter, power quality, SVM, topology, filter design.*

1. INTRODUCTION

In recent years, multilevel inverters are attracting the attention for high voltage, high power applications due to their superior performance compared to two-level inverters [1] .It is well known two-level inverters waveforms are not smooth as the multilevel inverters as multilevel inverters produce staircase output waveforms, smaller common voltage, draw low distortion input currents, operate at lower switching frequencies and posse high operating voltage capability [2], [3].

The most recently used inverter topologies are diode-clamped (neutral-clamped), capacitor-clamped (flying-capacitors), and cascaded multi-cell inverters. Among these topologies, cascaded multilevel inverter reaches the higher output voltages and power levels (13.8KV, 30 MVA) and the higher reliability due its modular topology. Even these merits they have limits including higher no. of semiconductor switches required adds more complexity to the layout, isolated voltage sources may not always be available[4],[5].It is considered that for low and medium voltage applications in range of (400 V – 5.5 KV); it's too expensive to build a high level inverter. It's recognized that up to 5-level would satisfy the convenience between power quality and economic considerations.

There are various modulation techniques such as SPWM, SHE, SVPWM.SVM is a digital modulation technique firstly applied for two-level inverters and then extended to multilevel inverters. Choi was the first author to extend the two-level SVM technique to more than three levels. SVPWM is considered the optimal technique as: i) It has the highest dc link voltage utilization ratio, reducing commutation losses and THD; ii) It is suitable for digital signal processing (DSP) implementation with optimal switching patterns as well [6], [7]. A lot of algorithms have been presented during last years [8 - 11]. The worked scheme is based on a simple SVPWM algorithm proposed by Gupta [7], [12]. Passive filters are used to compensate the harmonic distortion and the reactive power [13].An LC filter is designed to reduce the THD according to IEEE limits. This paper gives a comparative study for 3-level and 5-level of a

cascaded H-bridge inverter showing THD minimization using LC filter. An Induction motor is considered as a standalone load. The whole control system is implemented using MATLAB/SIMULINK.

2. INVERTER TOPOLOGY

The popular topology of cascaded multilevel inverters is shown in Figure 1 and figure 2. The circuit of figure 1 represents the three-level inverter and employs 12 power switching devices in 3 cells with separate dc-bus voltage for each cell. The same for the circuit of figure 2, it represents the five level inverter and employs 24 power switching devices in 6 cells "every 2 cells represent a leg of one phase" with separate dc-bus voltage for each cell.

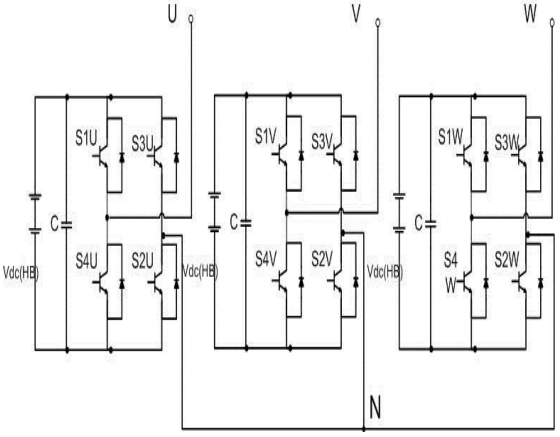

Fig. 1 Three level inverter.

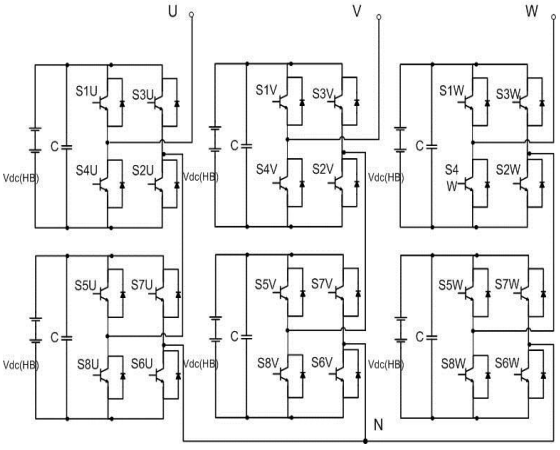

Fig. 2 Five level inverter.

3. SPACE VECTOR PWM

The concept of space vector modulation is derived from rotating field of AC machine which is used for modulating the inverter output voltage. The three phase quantities can be transformed to their equivalent 2-phase quantity either in synchronously rotating frame (or) stationary frame [14].

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (1)$$

The space vector diagram of a three-phase voltage source inverter is a hexagon, consisting of six sectors as shown in fig.3.

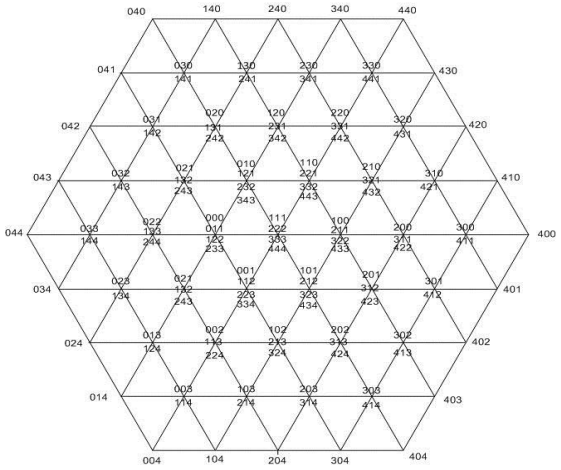

Fig. 3 Space vector diagram.

The algorithm in steps is: i) identify the triangle in which the point P is located, ii) then using the small vector analogy in the virtual two-level geometry; the on-times for this triangle can be calculated, iii) For optimal switching sequence, voltage vectors should be chosen to decrease the number of switching when transferring from states to another to decrease thermal stresses on active switches.

Here, the operation is explained for the first sector, the same is applicable for other sectors too.

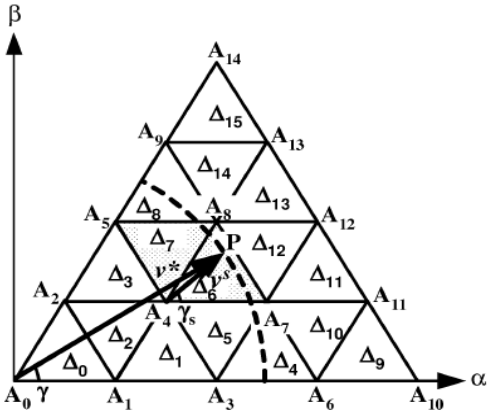

Fig. 4 First sector of the space vector diagram.

The search for the triangle that has point P can be obtained by using two integers k_1 and k_2, which are dependent on the coordinate (v_α, v_β) of point P as [12]:

$$k_1 = int\left(v_\alpha + {}^{v_\beta}/_{\sqrt{3}}\right) \quad (2)$$

$$k_2 = int\left({}^{v_\beta}/_{h}\right) \quad (3)$$

The cascaded inverter is simulated using Matlab/Simulink and the following results of voltage and current waveforms of both 3-level and 5-level inverters are obtained.

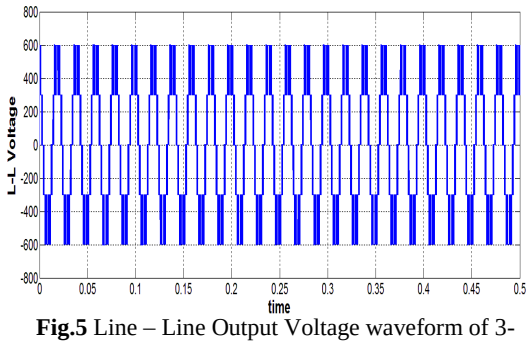

Fig.5 Line – Line Output Voltage waveform of 3-level inverter.

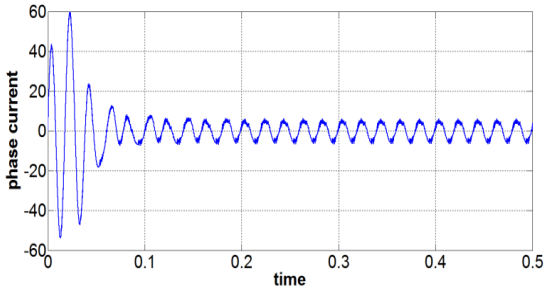

Fig.6 phase current waveform of 3-level inverter.

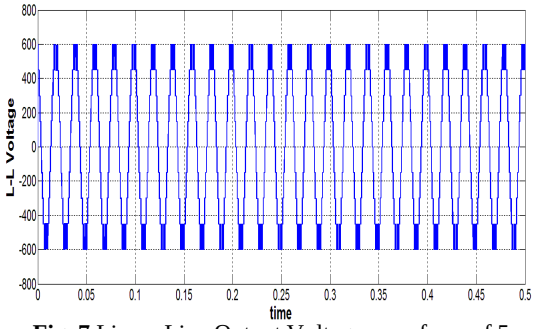

Fig. 7 Line – Line Output Voltage waveform of 5-level inverter.

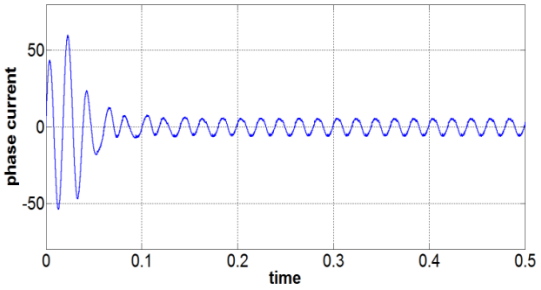

Fig.8 phase current waveform of 5-level inverter.

The special feature of multilevel inverters is that when the number of levels is increased; it reduces the THD.This feature is illustrated in these results which show the great difference of THD values between 3-level and 5-level inverters.

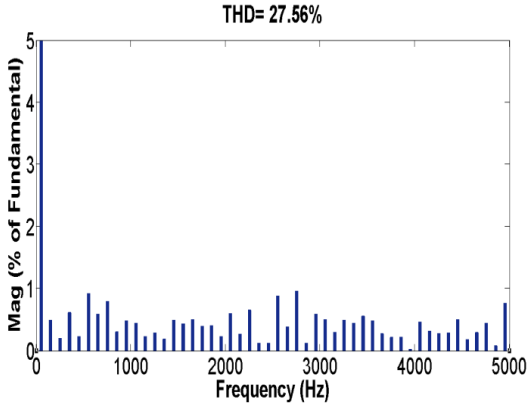

Fig.9 THD value of the Output Voltage waveform of 3-level inverter.

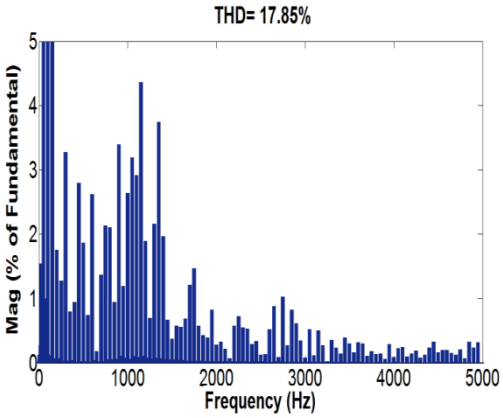

Fig.10 THD value of the current waveform of 3-level inverter.

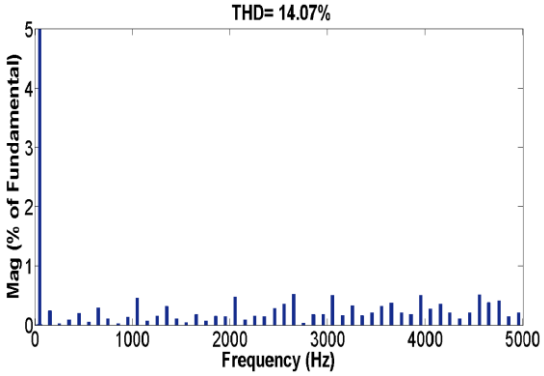

Fig. 11 THD value of the Output Voltage waveform of 5-level inverter.

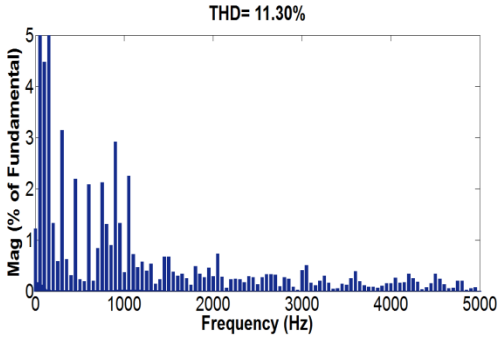

Fig.12 THD value of the current waveform of 5-level inverter.

4. HARMONIC LIMIT STANDARD

In order to prevent the system waveform from the distortion, a number of harmonic limit standards are exist for system operators and electricity producers to keep the high power quality. The limits depend on the system specifications, such as voltage level and power level.

According to IEEE standards "IEEE std. 519 -1992"; the recommended voltage distortion limits are shown in table [15].

These limits should be used as system design values for the worst case for normal operation. For shorter periods, during start-ups or unusual conditions, the limits may be exceeded by 50 %.

TABLE.1: Voltage Distortion Limits

Bus Voltage at PCC	Individual Voltage Distortion (%)	Total Voltage Distortion THD (%)
69 kV and below	3.0	5.0
69.001 kV through 161 kV	1.5	2.5
16.001 kV and above	1.0	1.5

Even this great decrease of THD value for 5-level inverter; these results are exceeding the "IEEE std. 519 -1992" limits. This problem can be fixed by increasing the no. of levels or using a passive filter. Since the control is more complex in higher levels; Hence, the need to use a passive filter to improve the system performance.

5. LC FILTER DESIGN

LC filters are used to attenuate the harmonics. LC-filter has one inductor in series and one capacitor connecting in parallel with inductor. To design the filter, some limits on the parameter values should be considered [16], [17].

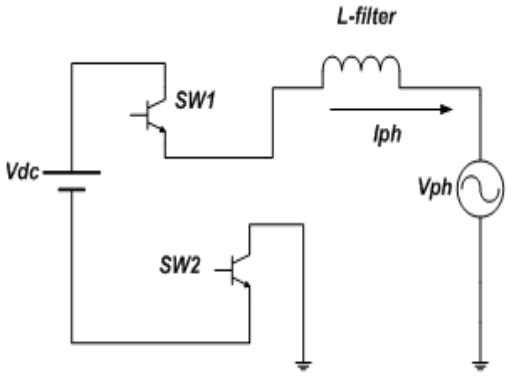

Fig. 13 CMI simplified circuit

To design the filter inductor [18]; the multilevel inverter circuit can be simplified to a buck chopper in figure 13.It's operation is determined according to its switching frequency, the conventional voltage equation of any inductor is

$$V_l(t) = L\frac{di(t)}{dt} \qquad (4)$$

This equation can be re-written according to the circuit shown as;

$$L_{filter} = \frac{V_{dc}-V_{ph}}{2\,\Delta I_l}\cdot DT_s \qquad (5)$$

As the current ripple is maximized at duty cycle of 0.5 (the worst case); the equation of filter inductance is:

$$L_{filter} = \frac{V_{dc}}{8\,f_{sw}\,\Delta I_{lmax}} \qquad (6)$$

The filter inductor must be able to limit the ripple at the output current to 10% of the rated amplitudevalue. The capacitor value is calculated through a percentage (x) of the reactive power absorbed at

rated power which indicates to the power factor. It is considered that the maximum power factor variation seen is 5%; however, values > 5% can be used [19]:

$$C_f = x.C_b \;\; ; \;\; 0.05p.u < C_f < 0.1p.u \qquad (7)$$

Passive damping must be sufficient to avoid oscillation; the damping resistor can be calculated [18];

$$R_d = \frac{1}{3*w_{res}*C_f} \qquad (8)$$

Parameter values of LC filter Design for multilevel inverter connected with IM

TABLE.2 System parameters	
V_{dc}	300 V
f_{sw}	3.6 KHz
$V_{n(L-L)}$	400 V
P_n	5 KW
f_n	50 Hz
L_f	$5.08 * 10^{-3}$ H
C_f	$5 * 10^{-6}$ Farad
f_{res}	1 KHz "within limits"
R_d	10 ohm

The THD of the Output voltage for both 3-level and 5-level inverters connected to Induction Motor are reduced to safe values as shown in the following Matlab/Simulink results:

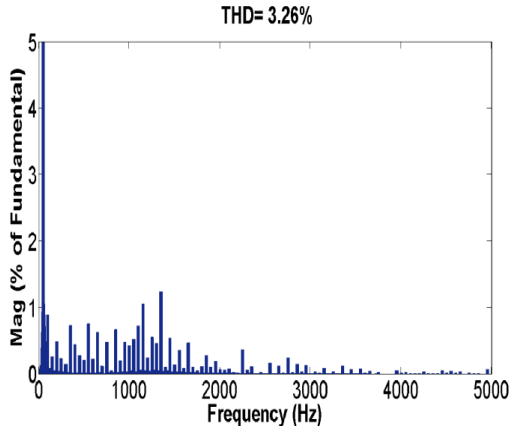

Fig.14 THD value of the Output Voltage waveform of 3-level inverter using LC-filter.

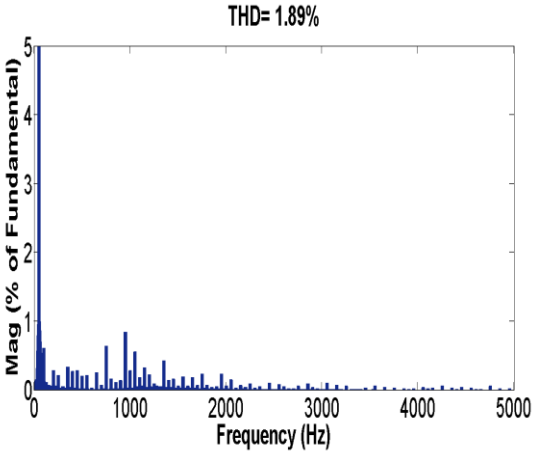

Fig.15 THD value of the Output Voltage waveform of 5-level inverter using LC-filter.

Consequently the current profile drawn by the induction motor is enhanced; the following results of current waveforms and THD for 3-level and 5-level inverters using Filter shown in Figures approve this enhancement.

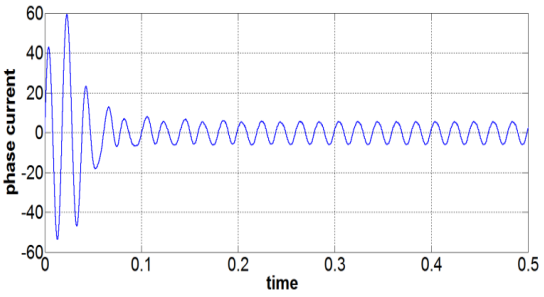

Fig.16 phase current waveform of 3-level inverter using filter.

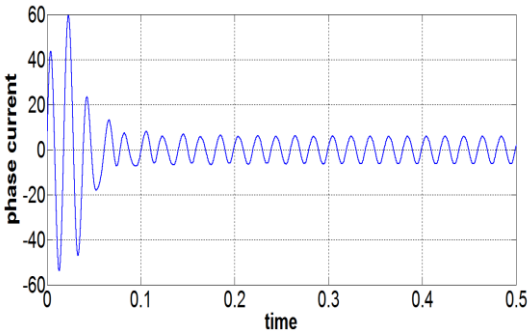

Fig.17 phase current waveform of 5-level inverter using filter.

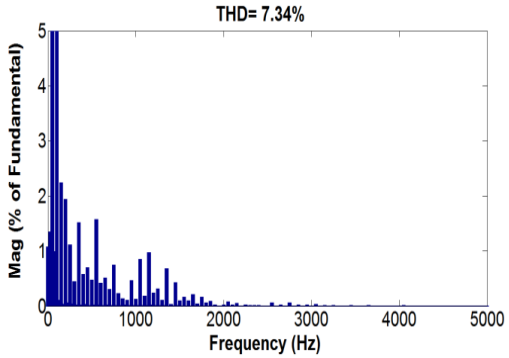

Fig.18 THD value of the current waveform of 3-level inverter using LC-filter.

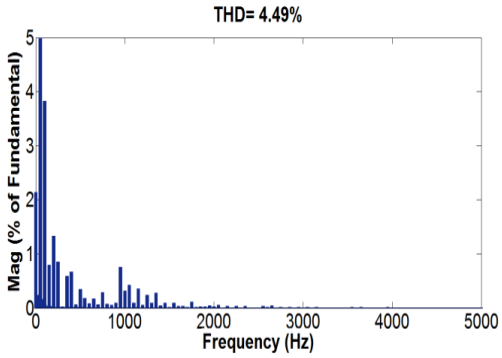

Fig.19 THD value of the current waveform of 5-level inverter using LC-filter.

The speed curves of the motor for both inverters are shown in the following results;

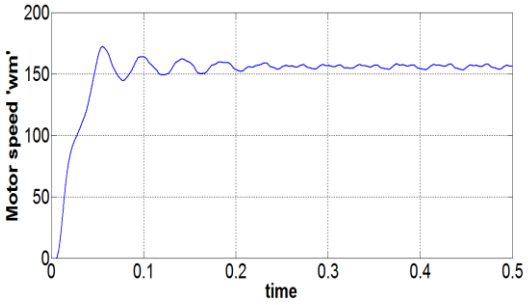

Fig.20 Speed curve of Induction Motor connected to 3-level inverter.

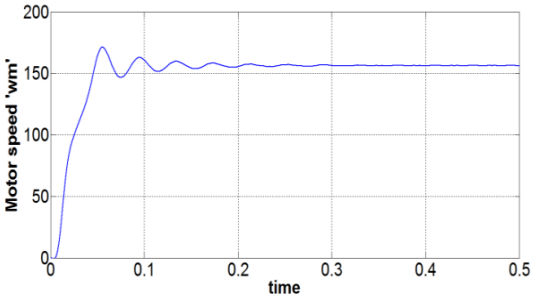

Fig.21 Speed curve of Induction Motor connected to 5-level inverter.

6. ANALYSIS OF RESULTS

Table.3 compares the obtained results of output voltage and current waveforms and shows the effect of adding the filter for these multilevel inverters. From this table, the output voltage THD values have improved from 27.56% to 3.26% for 3-level inverter and from 14.07% to 1.89% for 5-level inverter.

TABLE.3: Comparison between THD values for each inverter

	Voltage THD "without filter"	**Voltage THD "with filter"**	**Current THD "without filter"**	**Current THD "with filter"**
3-level	**27.56 %**	**3.26 %**	**17.85 %**	**7.34 %**
5-level	**14.07 %**	**1.89 %**	**11.30 %**	**4.49 %**

7. CONCLUSION

This paper has presented a detailed analysis of 3-level and 5-level inverters with an induction motor as a load to improve their performance. SVM is applied to the CMI. It has approved the senior property of multilevel inverters as the THD has been reduced by increasing the number of levels. The damped filter has been carefully designed to attain the THD to standard safe limits typically 5%. Using this filter; the measured values of THD obtained with Matlab/Simulink are 3.26% for 3-level inverter and 1.89% for 5-level inverter. It is remarked that a considerable reduction in the voltage THD has been attained; also the current profile of the motor has been enhanced due to the presence of this damped filter. It has been concluded that for higher levels, power quality has improved and filter size has reduced. Despite these distinct advantages, there is a limitation for the number of levels for low and medium voltage drives due to the large expenses of the additional components, so it's convenient to use multilevel inverters up to 5-levels for such a drive.

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