A CLOSE ACCORD ON DFT BASED FREQUECY AND PHASOR ESTIMATORS USED IN NUMERICAL RELAYS

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Abstract: ***In this paper, a close accord on the Discrete Fourier Transform (DFT) technique based frequency and phasor estimations for protective numerical relays application is presented. The effectiveness of the recursive DFT, in particular, is examined via simulation corroborated by experimental verification. Possibility of error accumulation in the estimated magnitude by the recursive DFT is highlighted and novel solutions are proposed. Impact of different input signal patterns on the algorithms' performance is further examined. In addition, effect of rate of change of input signal frequency on the estimated values is pinpointed. The testing circuit hardware is implemented using the digital signal processing technology. The results of this study are greatly valuable for the protection engineers particularly those concerned with the development and implementation of numerical relays.***

Keywords: *Discrete Fourier Transform (DFT), Phasor and frequency estimation, Digital signal processing, Computer relaying.*

I. INTRODUCTION

The interests and investments in power system numerical relays are increasing rapidly in the recent years. Numerical relays offers the utility with a programmable, reliable, flexible and multi function protection devices that guarantee secure and selective fault detection and correct isolation. Recently, the relay functions have been extended to provide control, metering, monitoring, and disturbance and event recordings. Thus, accuracy of the measuring element of numerical relays is highly important.

Most of the measuring elements of numerical relays are based on one or more digital filter algorithm to extract the rms value of the input signal. The DFT filter represents the most important technique used for fundamental and harmonic measuring as reported in various publications [1-4]. DFT filter has been introduced in two forms; non-recursive and recursive. The lower mathematical operations of the recursive form compared to the non-recursive are considered an evident for the common use of the recursive one. Also, many development have been proposed to adapt the recursive DFT for frequency measuring in stead of conventional methods such as zero crossing and phase locked loop (PLL) as it

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reduces the hardware required. In addition, the recursive form [illegible]
adaptive sampling rate application [2-4]. Therefore, most of the developed industrial relays are based on the recursive form. Unexpectedly, it has been reported that the conventional methods such as zero crossing, PLL, ... etc. in addition to recent reported demodulation technique would produce during power system dynamics better frequency tracking than that obtained using the recursive DFT [5-7]. No evidence has been given in the simulation study to explore the reason(s) of the poor performance of the recursive DFT during frequency dynamics. In order to sort out these contradictions, a deep investigation of the DFT tested with different patterns of input signal is required. Also, there is no sufficient material published on the behavior of the frequency and phasor estimators during step change in the input signals, presence of sub and non-synchronous harmonics, dc decaying, ... etc. Moreover, the experimental phase in most of the aforementioned studies is absent. These issues in addition to the explanation of the poor performance of frequency algorithm during dynamics will be addressed in this paper.

In this paper, a close accord on the DFT technique used for frequency and phasor estimations is presented. The behavior of the estimators during sudden application of the input signals, sub and non-synchronous harmonics, dc decaying, ... etc. is outlined. Explanation of the poor performance of the recursive DFT used in frequency measurement during dynamics is highlighted. This study is performed via Matlab simulation corroborated by experimental setup. The set-up consists of a DSP board interfaced with MIO board. Details of the study are given in the following sections.

II. DESCRIPTION OF EXAMINED ALGORITHMS

A) DFT Filter Equations

In order to extract the fundamental component of an input signal samples (X_j), a full cycle DFT filter in its non-recursive form can be applied according to the following forms [1]:

$$C = \frac{2}{N}\sum_{j=1}^{N} X_j \cos(\frac{2\pi j}{N}) \qquad (1)$$

$$S = \frac{2}{N}\sum_{j=1}^{N} X_j \sin(\frac{2\pi j}{N}) \qquad (2)$$

where S and C are the sine and cosine terms of the phasor and N is the number of samples per cycle. The magnitude of the peak value (F) and the phase angle (Φ) are given by:

$$F = \sqrt{S^2 + C^2} \qquad (3)$$

$$\Phi = \tan^{-1}(\frac{C}{S}) \qquad (4)$$

It has been proved earlier that the estimated phasor by the non-recursive DFT is rotational in the complex plan as the angle Φ is successively increased as the data window moves to the new sample by an angle (θ) where θ is equal to $2\pi/N$.

B) Recursive DFT as a Phasor Estimator

On the other hand, the computed phasor by the recursive DFT (F_j) is stationary in the

complex plan. This simplifies the correlation of power system phasor with the estimated one by the recursive form as [1-5]:

$$C_j = C_{j-1} + \frac{2}{\mathrm{N}}\cos\left(\frac{2\pi j}{N}\right)\left(X_j - X_{j-N}\right) \tag{5}$$

$$S_j = S_{j-1} + \frac{2}{\mathrm{N}}\sin\left(\frac{2\pi j}{N}\right)\left(X_j - X_{j-N}\right) \tag{6}$$

$$F_j = F_{j-1} + J\frac{1}{\sqrt{2}}\frac{2}{\mathrm{N}}\left(X_j - X_{j-N}\right)e^{\frac{-2\pi j}{N}} \tag{7}$$

and the angle Φ can be determined by a similar form to that given in Eqn. (3). Note that, F_j equals to F_{j-1} as long as the sample X_j equals to X_{j-N}.

C) Frequency Measurement Algorithm

The frequency deviation measurement is based on the angular displacement of the estimated phasor by the recursive DFT. The algorithm is inherently insensitive to harmonics because of the filter characteristics of the DFT, but it is vulnerable to noise, and requires long measurement windows when frequency deviation from nominal is small. If the input signal frequency is assumed to change slightly from $50Hz$ by an amount (Δf), while the sampling clock frequency remains fixed, the estimated phasor $F'_{(50+\Delta f)}$ can be correlated to the original one $F'_{(50)}$ as [1]:

$$F'_{(50+\Delta f)} = F'_{(50)}\frac{\sin\left(\frac{\pi\Delta f}{50}\right)}{\mathrm{N}\times\sin\left(\frac{\pi\Delta f}{50\,\mathrm{N}}\right)}\times e^{J\frac{2\pi\Delta f r}{50\,\mathrm{N}}} \tag{8}$$

where r is the recursion number. It is evident from Eqn. (8) that the phasor obtained recursively undergoes two modifications in the magnitude and phase by factors ΔF and $\Delta\Phi$, respectively. These factors are given by:

$$\Delta F = \frac{\sin\left(\frac{\pi\Delta f}{50}\right)}{\mathrm{N}\times\sin\left(\frac{\pi\Delta f}{50\,\mathrm{N}}\right)} \tag{9}$$

$$\Delta\Phi = \left(\frac{2\pi.\Delta f.r}{50\,\mathrm{N}}\right) \tag{10}$$

It is evident from Eqns. (9) and (10) that the magnitude factor is independent of r and is relatively small for small changes in frequency. However, the change in the phase angle is far more sensitive to the Δf, and provides a most direct measure of frequency. Thus, the phase angle at rth recursive computation depends directly upon the frequency deviation and the recursion order r. Since r increases by one in each iteration, the recursive relation for Φ_r can be represented by:

$$\Phi_r = \Phi_{r-1} + \frac{2\pi\Delta f}{50\,\mathrm{N}} \tag{11}$$

Eqn. (11) would give direct measure of the frequency deviation by estimating two consecutive values of the phase angle Φ taking the initial assumption that the time

interval between two iterations ($1/50N$ s) is constant. Then, the on-line value of the frequency (f) can be calculated by:

$$f = 50 + \frac{1}{2\pi} \frac{\Phi_r - \Phi_{r-1}}{\frac{1}{50N}} (Hz) \qquad (12)$$

Note that, when the input signal frequency is higher than $50Hz$, the phasor rotates in the counter clockwise direction, i.e $\Delta\Phi_r$ is positive. Whereas for an input signal frequency with lower frequency than the nominal, the phasor rotates in a clockwise direction, i.e. $\Delta\Phi_r$ is negative. Two issues had been early raised during the real time realization of Eqn. (12) leading to sensible reduction in the algorithm performance. These are the measurement of Φ_r and the mathematical precision particularly when Δf is small i.e. $\Delta\Phi_r$ is very small. The first problem has been eliminated with the application of new generations of microcontrollers and DSP's having a powerful mathematical instruction list with at least 16-bit word width. However the second problem, which is related to the computation precision, is still the major problem challenging this technique to be dominated. Thus, estimation of f is usually performed with much care to avoid false indication.

III. TESTING OF ALGORITHMS

In order to evaluate the algorithms' effectiveness and explore the reasons for the poor performance of the frequency algorithm during dynamics, extensive tests are performed using computer simulations. The Matlab software has been employed in the phase of simulation and the algorithms response have been recorded for different input signal equations. However for real time evaluation, experimental tests of new algorithms or relays is usually carried out in the laboratory employing the flexibility of digital computer simulation as recommended recently by the IEEE committee [8,9]. In these simulations, the currents and voltages waveforms taken from a computer simulation or digital fault recorder are converted into analog signals, amplified and then fed to the tested hardware. This procedure would overcome the difficulties involved in fault-throwing tests that carried out on a real power system. Description of the laboratory testing setup is given in the following section.

A) Tester Setup

The tester setup consists mainly of the DSP board DS1003 interfaced with multi-I/O board DS2201, as shown schematically in Fig. 1 [10]. The DS1003 board is based on the Texas Instruments TMS320C40 floating-point DSP. The DS2201 facilitate the interfacing with the real system through 20 simultaneous analog input channels (distributed to 5 A/D converters), 8 analog output channels (distributed to 2 D/A converters), and a 16-bit general purpose digital I/O port. A personnel computer (PC) was employed as a host machine for storing and downloading the program software. Also, it facilitates monitoring and plotting the selected variables during real time using the TRACE software [11].

The recursive DFT and the frequency measuring algorithms are constructed depending on the Eqns. (1-12) considering the instructions for the DS1003 software environment. In which, the corresponding algorithm is developed by the high level language including individual algorithms of the DFT and frequency estimators. Then, the programs are

compiled using Texas Instruments TMS320C40 C-compiler/Assembler/Linker and then downloaded to the DS1003 local and global memories. A brief description of the main parts of the implemented algorithm is given below.

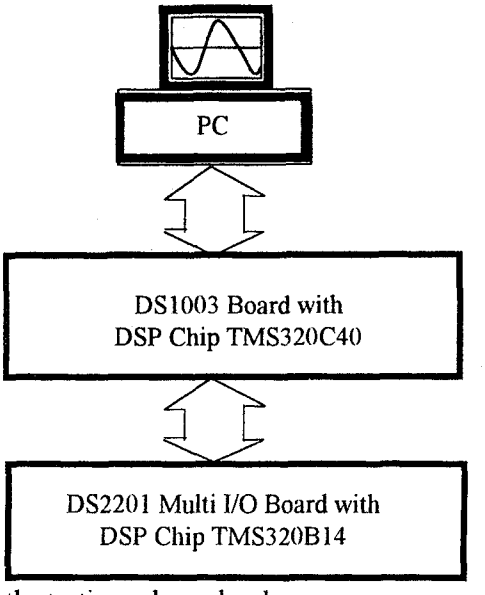


Fig.1. Schematic diagram the testing scheme hardware

B) Implemented Real-Time Algorithm

The main parts of the implemented real time algorithm are the off-line and on-line parts.

Off-line Algorithm: In which, the implemented hardware should be initially set according to the initialization steps of the DSP board. Also, the selected sampling interval is declared 625μsec, which is equivalent to sampling rate of 32 sample per cycle. This stage also includes the declaration of the sine and cosine coefficients of the DFT tuned on the fundamental components of 50*Hz*. In addition, the parameters of the frequency estimator and the scaling factors are declared.

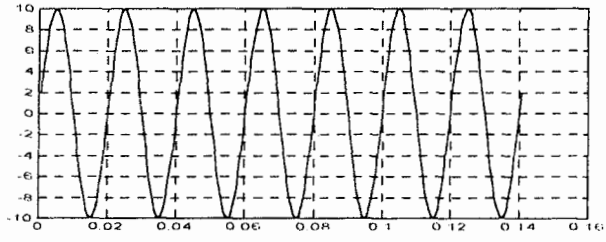
On-line calculation: This part of the algorithm is concerned with all calculations that are simultaneously executed at each sample. It includes generation of the testing signals, scanning of the input signals, DFT and frequency algorithms, and variable tracing.

1. ***Testing Signals Generation:*** Two different sources are used to generate the testing signals. Signals with stationary frequency and magnitude are generated by a signal generator and fed directly to the analog input port of the DS2201. However, signals associated with dynamics such as dc decaying, harmonics, frequency deviations ... etc. are generated using computer simulation. The DSP TMS320B14 of the multi input/output board is programmed to function in the slave mode to generate these dynamic testing signals. These signals in the digital form are converted into analog pattern via on board *D/A* converter. The signals are defined in the program in an either analytical equation(s) in the discrete form or vector of data. These data are usually extracted from power system simulation software such as the Electromagnetic Transient Program (EMTP) or fault recorders. Then, it is scaled down to suit the DS2201 operation limits. The analog signals are then fed to the phasor and frequency estimators implemented on DS1003 hardware. This testing procedure is similar to that one reported in [12,13]. Based on this testing procedure, the developed schemes were checked through different fault cases, system dynamics, frequency drift, ... etc.

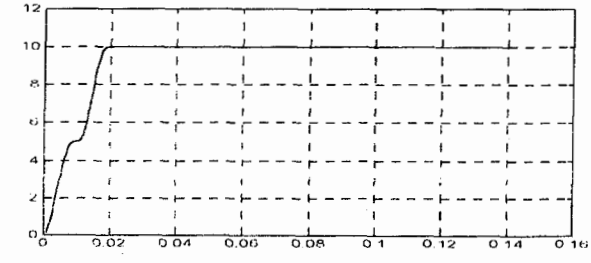
2. ***A/D Conversion***: The selected analog input channels are sampled and the inputs are converted through the *A/D* converters into their digital form.
3. ***Estimators' Algorithm***: The recursive DFT and the frequency estimators are implemented according to Eqns. (1-12). These estimators are fed with the sampled input signal. Either one or all estimators can be enabled to evaluate the response in a comparative manner.

IV. TEST RESULTS

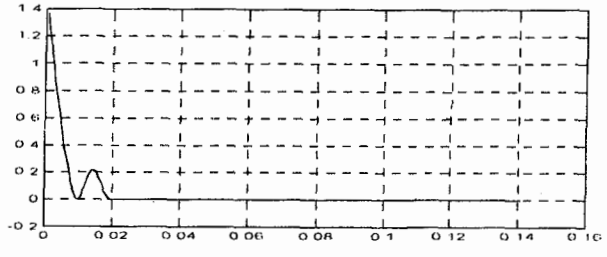
The recursive DFT filter coefficients are tuned with the 50*Hz* signal and the estimators are exposed to variable patterns of input signals. Fig. 2 shows the Matlab simulation results for the DFT and frequency algorithms output for typical 50*Hz* input signal. However, Fig. 3 shows the experimental measurement for the same stationary input.



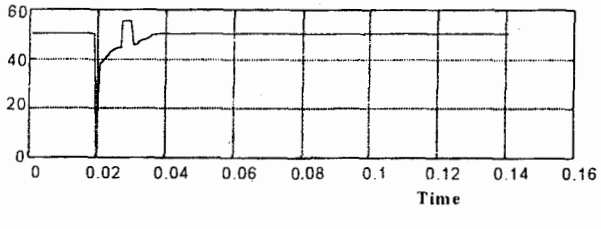
(a) Input signal



(b) Magnitude



(c) Phase

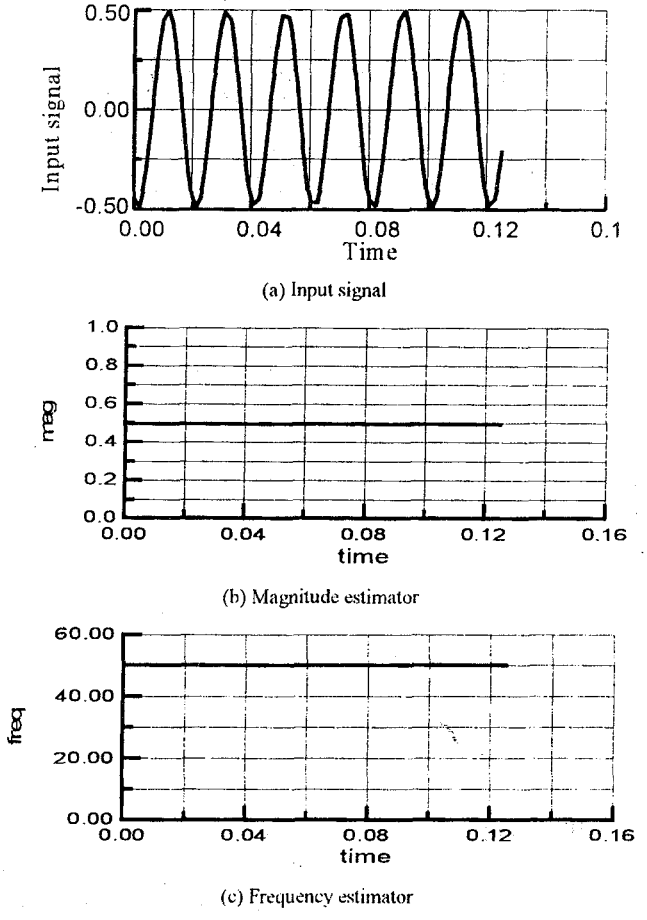


(d) Frequency

Fig. 2. Recursive DFT and frequency estimators for 50*Hz input*

Note that, all frequency measurements in this paper performed by the hardware setup are obtained via averaging 32 values of frequency deviations over the cycle, which is added once at the end of the cycle to the original frequency. Also, analog input signals are traced in the presented figures in a scaled down range of ±1.0 corresponding to ±10.0 of the A/D converter reference voltages. It is evident from Figs. 2 and 3 that the performances are similar. The transient appears in Fig. 2 in magnitude, phase, and accordingly the frequency is due to the starting of the application of the input signal. However, the experimental results given by Fig. 3 are recorded few cycles post-input signal application. Therefore due to this similarity of results, the rest of figures presented in this paper are the experimental ones only.

The dc decaying has a considerable influence on the performance. Both frequency and magnitude estimators are behaving with transient errors over the period of the dc decaying time constant (τ). In Fig. 4, the input signal magnitude is switched from $0.2V$ to $0.5V$ superimposed with dc decaying signal of $0.25V$ and τ is $0.1s$. It can be seen that the transient error associated with frequency estimator is more significant than that of the magnitude estimator particularly with τ value is relatively high; 5 times the cycle period. Fig. 5 shows the schemes response for the fundamental input signal of $0.5V$ amplitude superimposed with $0.25V$ and $30Hz$ signal. Wide swinging band in the estimated magnitude indicates the serious impact of the sub-synchronous frequencies on measuring



(a) Input signal

(b) Magnitude estimator

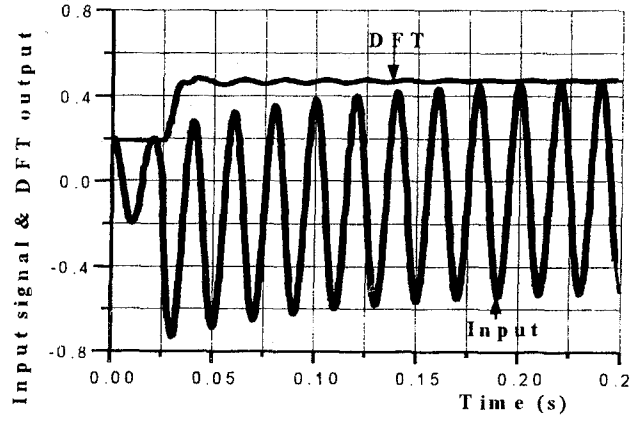
(c) Frequency estimator

Fig. 3 Recursive DFT and frequency algorithms for $50Hz$ input.

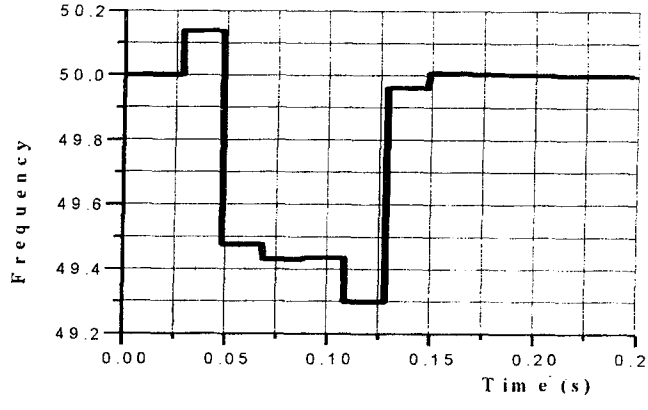
frequency and ±20% in the magnitude from the original values. This would adversely affect relay operation particularly with instantaneous units excited by the estimated signals. However, Fig. 6 shows the schemes response for input signal of 50.4*Hz* and 0.5*V* amplitude. Deviation of 0.4*Hz* in frequency exhibits natural reduction in the estimated magnitude due the DFT frequency response, however the estimated frequency is fairly accurate.

V. ERRORS ACCOMULATION BY RECURSIVE DFT

During the phase of the experimental work of this paper, a figure of limit cycle with low frequency (few or fraction of Hertz) has been recorded for the estimated magnitude based on recursive DFT even with input signals have frequencies very close to the 50*Hz*. These limit cycles or oscillations have been never recorded with that considerable magnitude for the non-recursive DFT in miscellaneous applications [12,13].



(a) Input signal and magnitude estimator output

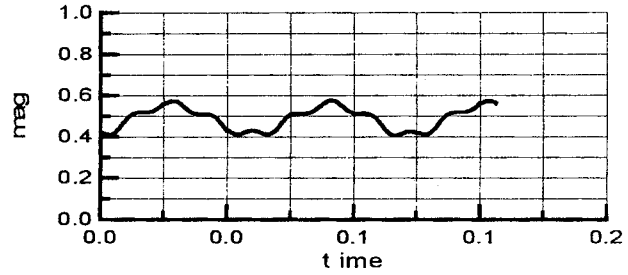


(b) Estimated frequency

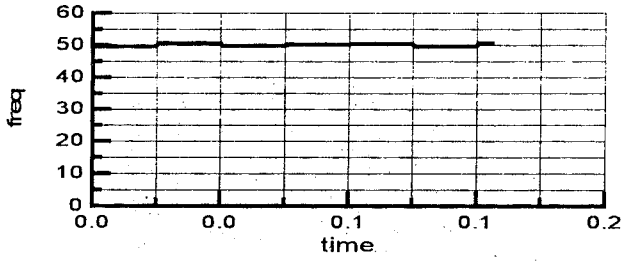
Fig. 4. Effect of the exponential decaying superimposed signals.

Usually these oscillations amplify the overall produced error in the estimated magnitude. Fig. 7 represents one of these cases with the magnitude showing a limit cycle of 0.003*Hz* for a sinusoidal input derived from the 50*Hz* mains with 0.5 pu amplitude. The maximum error is 5%, which indicates considerable reduction in the efficiency of the estimator.

However the serious effect of the limit cycle is that it may lead into algorithm instability at some specific patterns of input signals or input conditions; i.e. the error will be magnified as shown by Fig. 8. In which, the input signal frequency was deviated to 49.9*Hz* and the associated limit cycle frequency is of 0.0011*Hz* has been established leading to estimator instability. Probability of magnified errors would be also increased with random noise signals superimposed to the non-perfect 50*Hz* signals such as the system mains. This shortcoming in the recursive DFT performance would explain why some industrial relays are still using the non-recursive form of the DFT [14].

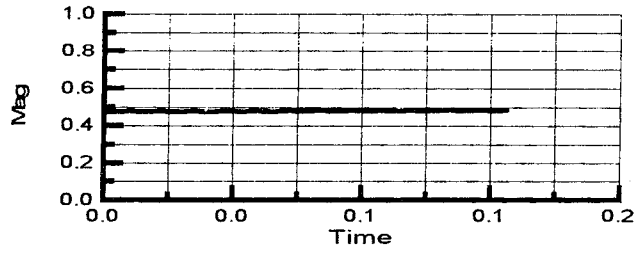


(a) Magnitude estimator.

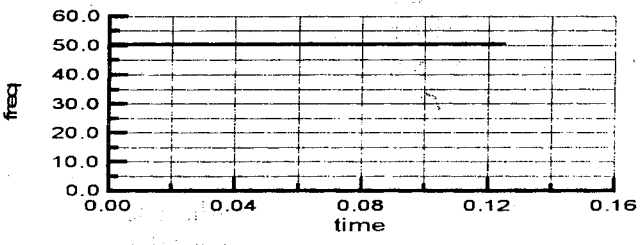


(b)Frequency estimator

Fig. 5 Effect of 30*Hz* superimposed signal on the estimators' performances.



(a) Magnitude estimator



(b)Frequency estimator

Fig. 6. The estimators' response for input signal of 50.4*Hz*.

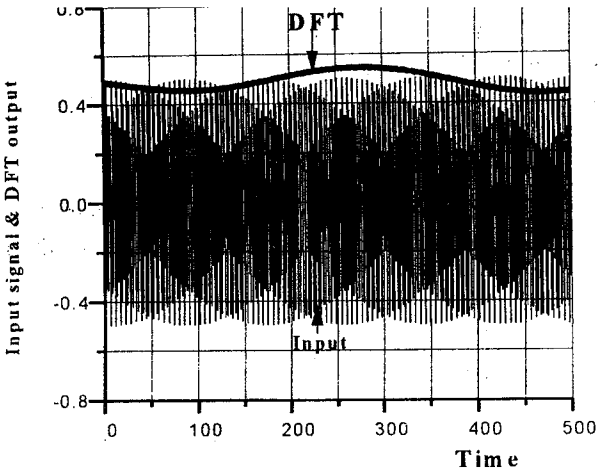


Fig. 7. The pattern of the limit cycles in the DFT output.

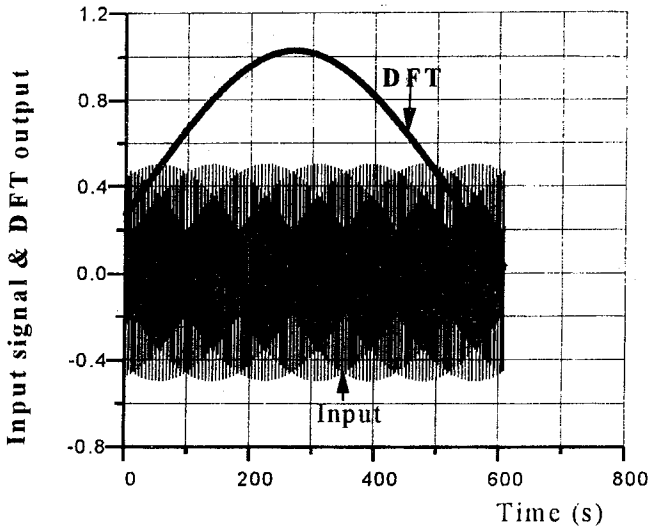


Fig. 8. Magnified limit cycle in the DFT output.

In fact, the generation of the low frequency limit cycle is expected according to Eqn. (8). Eqn. (8) described the deviation in the phasor parameters when the frequency is deviated by Δf. The generated limit cycle, which has Δf frequency, was the cause that leads to the rotation of the stationary phasor as given by Eqn. (10). However, the amplification of the limit cycle magnitude, adversely to Eqn. (9), is the issue that requires explaining. In order to fetch the reasons of this magnified error, several tests have been applied. It was apparently found that the recursive form itself of the DFT, acquisition, and quantisation errors would lead to this magnification. The recursive form inherently can not allow the technique to remove the computation errors, as they will be successively summed up. The acquisition errors (A/D converter and conditioning circuits' errors) can not alone produce these errors. This is because they are not recorded with the application of other algorithms such as the non-recursive DFT technique, which depicts these errors as jitters. Theoretically, this error should be self curing during real time implementation regardless of the used technique is recursive or non-recursive forms in one cycle period, if all computations are performed with no rounding or truncations. However with the

quantisation error (truncation and rounding of computed values to fit with the size of registers and memory addresses of the CPU.), limit cycle will be magnified. The proposed scenario for the magnification of the oscillations might occur is that dully acquisition errors produces quantisation error during the computation of the second term of Eqns. (4) and (5). This would lead to accumulation of errors due to the recursive form.

Definitely using the floating point DSP chip TMS320C40 with 32-bit memory addresses and 40-bit accumulator would highly reduce magnification of the limit cycle. However, the experimental measurements showed that the magnitude is still suffering from the effect of the limit cycle and surely the situation should be worst with processors having lower capabilities. Thus, in order to eliminate or highly reduce these limit cycles two applicable solutions are proposed. These are applying the side by side non-recursive DFT along with the recursive form or processing the recursive DFT using integer variable.

A) Side-by-Side Technique: In which the non-recursive and the recursive ones are executed in parallel according to the following:

1) The complete form of the recursive DFT is executed at each sample.
2) However, two terms (sine and cosine) only of the non-recursive DFT are computed at each sample. The terms are summed up over the cycle in two separate sine and cosine counters.
3) At the end of the cycle, the recursive DFT sine and cosine terms are updated with the non-recursive separate counters. Then, the non-recursive DFT counters are reset to zero. This yields that the magnitude computed over the cycle is obtained based on the recursive form and corrected every cycle with the non-recursive form.

   Towards the reduction of the mathematical operation required for the proposed side-by-side technique, Eqns. (5) and (6) are modified to be:

$$C_j = C_{j-1} + \frac{2}{N}\left(P_j X_j - P_j X_{j-N}\right) \qquad (14)$$

$$S_j = S_{j-1} + \frac{2}{N}\left(Q_j X_j - Q_j X_{j-N}\right) \qquad (15)$$

where P_j and Q_j are equal to $\cos(2\pi j/N)$ and $\sin(2\pi j/N)$, respectively. This yields no extra calculations for the non-recursive DFT except the addition operation as the components of the non-recursive DFT terms (P_jX_j and Q_jX_j) are implicitly computed. Fig. 9 shows the experimental measurement of the proposed side by side DFT output for an input of $0.5V$ and $49.6Hz$. In which, the limit cycles have disappeared and possibility of limit cycle error magnification has been eliminated even with higher frequency deviations.

B) Application of Recursive DFT Using Integer Variable: In this proposed procedure, DFT coefficients, received input samples, and DFT mathematical operations must be processed using integer format. The designer must be cautious that all the computation results do not exceed a pre-defined word size for each variable. Therefore, the scaling factors must be given a great care to avoid any overflow during computation. This proposed solution would prevent the error magnification and depict any acquisition error as bounded jitters. However, this solution would be recommended for integer point microprocessors only as it would involve many sophistication when applied to the floating point CPU's. Therefore, the proposed side-by-side technique is considered adequate to suite the operation of both integer and floating-point CPU's. Also, it gives trustful measuring of the magnitude even during random axis memory checksum errors as the

a recommended measuring element for protective relays.

VI. DEVIATIONS IN FREQUENCY ESIMATION

The frequency estimator algorithm effectiveness has been proven under step change in the original signal frequency. However, frequency fluctuation has a dynamical nature and therefore, the estimator should be examined under these conditions to verify its efficacy. Fig. 10 shows the effect of increasing the frequency by a rate of $1Hz/s$, without any change in the amplitude of the input signal. Big deviations in the estimated frequency were recorded and became worst for rate of change of $5Hz/s$ as given by Fig. 11. Also, the estimated amplitude is suffering from severe oscillations associated with considerable deviation in the measurement. This deviation is increased as long as the rate of change is increased. Concurrently, when the change in frequency is associated with a considerable change in the amplitude, which is similar to fault case, both frequency and phasor can have additional deviation particularly at the instant of change. This is recorded as shown by Fig. 12, where the magnitude estimator output is violently changing. However, for step change in the frequency, a lower deviation in the estimated frequency is obtained as shown in Fig. 13. This shows a better response of the frequency estimator in case of step frequency change than with ramp. This response is similar to second order system excited by different inputs; step of a change and ramp. This would be helpful if improvement of this algorithm is further targeted.

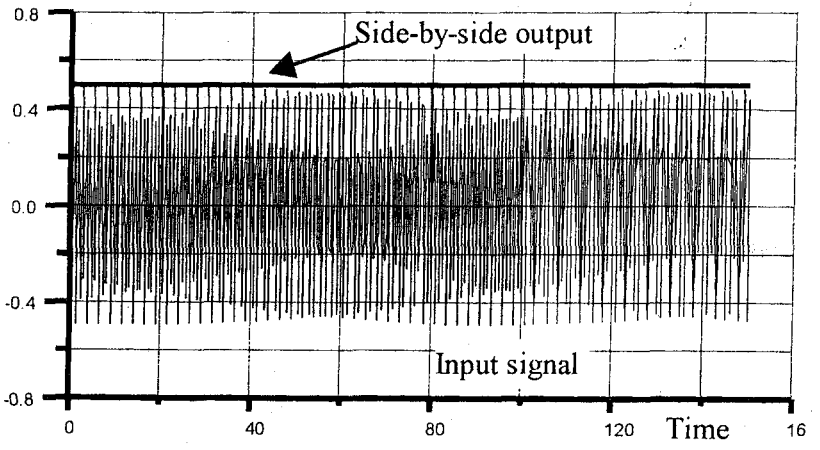
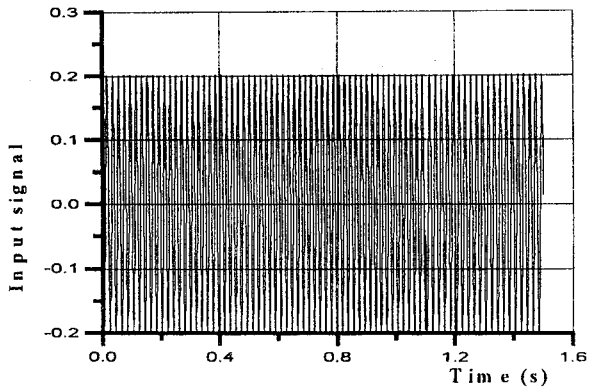
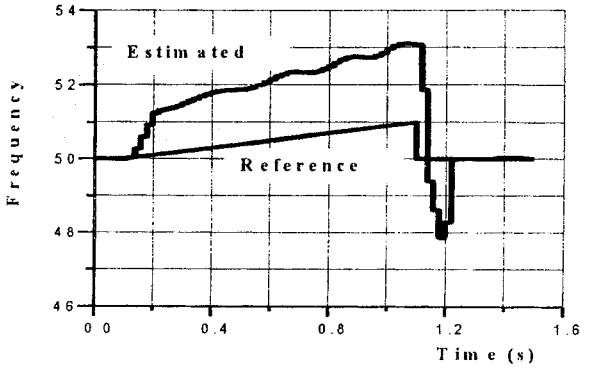


Fig. 9. Side-by-side DFT estimator response.

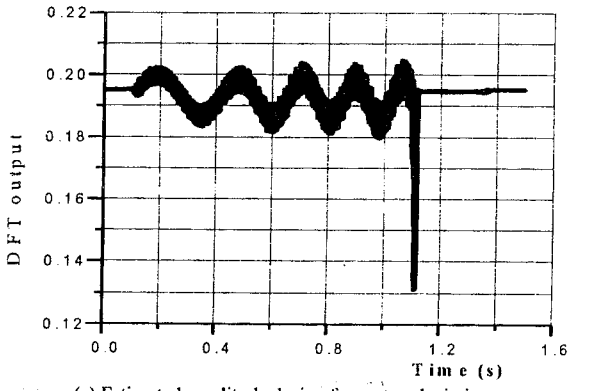
In fact these features are affecting the utilization of both frequency and recursive DFT estimators in numerical relays and must be cured. Relays such as overcurrent, over and undervoltage, directional elements, frequency ... etc. would loose either the security or sometimes the capability of fault detection. The side-by-side technique can highly improve the estimated magnitude for signals with fixed frequency. However during frequency deviations, slight improvement in the estimated magnitude can be observed with no sensible improvement in the estimated frequency can be recognized as shown by Fig. 14. This implies that the frequency algorithm is still behaving like a second order system with ramp input. Therefore, some sort of artificial intelligence technique can be applied to improve this technique, which would be an interesting subject of another investigation.



(a) Input signal with ramp drift in the frequency with 1*Hz/s*.

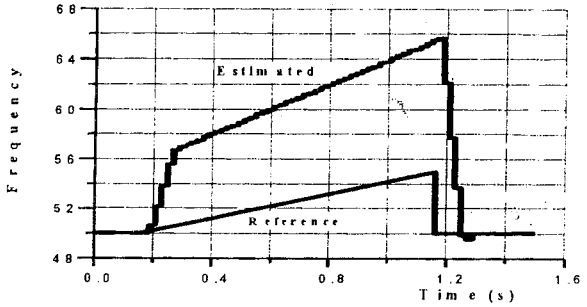


(b) Estimated frequency compared to the reference frequency.

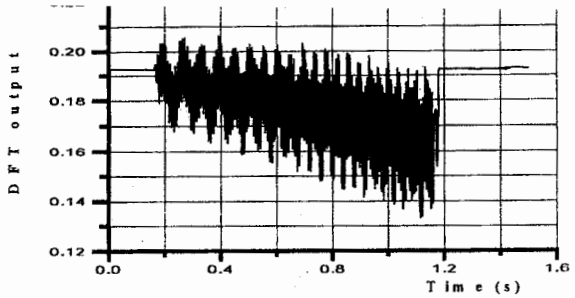


(c) Estimated amplitude during frequency deviations.

Fig. 10. Estimators' performances during frequency fluctuations of 1*Hz/s*.

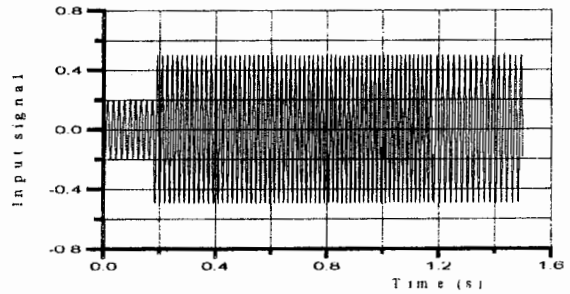


(a) Estimated frequency compared to the reference frequency.

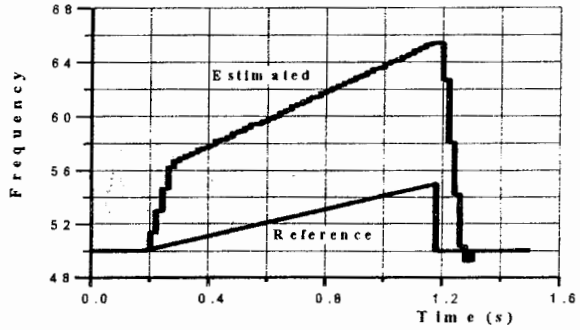


(b) Estimated amplitude during frequency deviations.

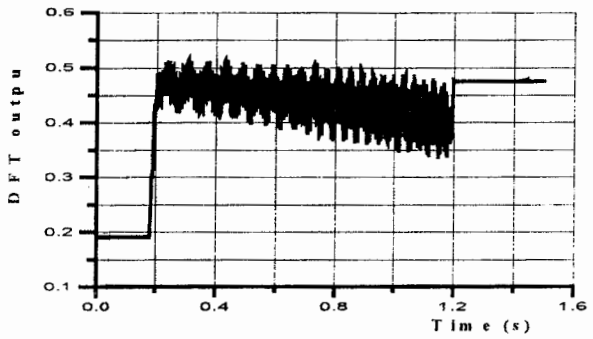
Fig.11. Estimators' performances during frequency fluctuations of 5.0*Hz/s*.



(a) Input signal with ramp change in the frequency with 5*Hz/s*.



(b) Estimated frequency compared to the reference frequency.



(c) Estimated amplitude during frequency deviations.

Fig.12. Estimators' performances during frequency fluctuations of 5.0*Hz/s*.

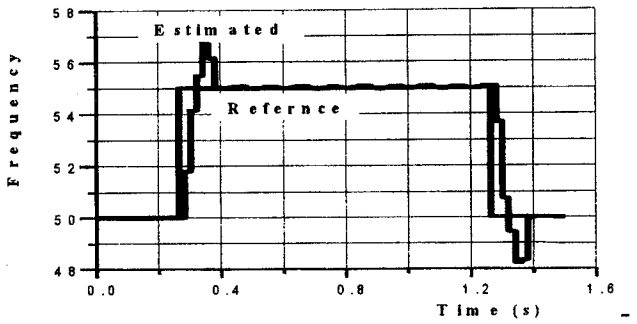
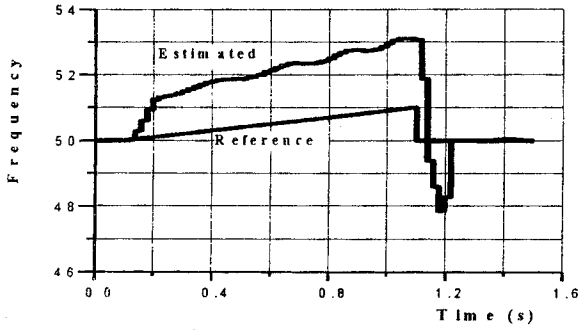
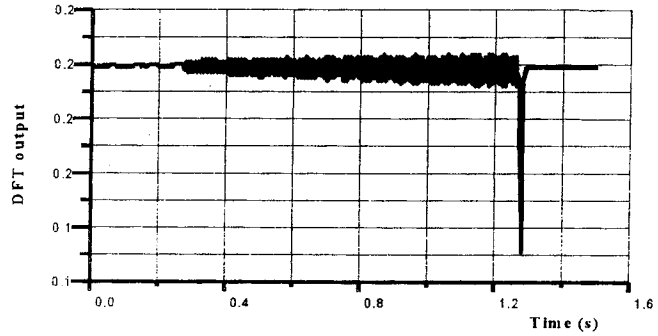


Fig. 13. Frequency estimator response for step change in frequency.



(a) Reference and estimated frequency



(b) Measured magnitude

Fig. 14. Side-by-side estimator response during frequency discrepancies.

VII. CONCLUSIONS

In this paper, a close accord on the Discrete Fourier Transform (DFT) technique used for frequency and phasor estimations has been introduced. The evaluation of the recursive DFT technique has been determined via simulation and validated by experimental verification. Possibility of error accumulation in the estimated magnitude by the recursive DFT has been recorded and possible practical solutions have been proposed. Effect of rate of change of input signal frequency on the estimated frequency and magnitude is pinpointed and a procedure for magnitude error correction is suggested. The testing circuit hardware is implemented using the digital signal processing technology. The paper results are valuable for the protection engineers particularly those concerned with the implementation of numerical relays.

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IX. BIOGRAPHY

Hatem A. Darwish was born in Menoufiya, Egypt, on September 13, 1966. He received his B.Sc., M.Sc., and Ph.D. degrees in Electrical Engineering, Menoufiya University, Egypt in 1988, 1992, and 1996; respectively. From 1994 to 1996, he was working towards the Ph.D degree at Memorial University of Newfoundland, St. John's, Canada based on joint supervision with Menoufiya University. In 1996, he was appointed as an assistant professor at Menoufiya University. He has been involved in different pilot projects for the design and implementation of digital relays and SCADA for medium voltage distribution systems for the Egyptian Industry. His current interests are in digital protection, signal processing, power system automation, and power system studies including hvdc transmission.

عنوان المقالة:

" دراسة مستفيضة لمرشح فورير مبنى عليه مقياسى التردد والمتجهات الكهربية المستخدم فى المتممات الرقمية "

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ملخص المقالة

تقدم المقالة دراسة مستفيضة لمرشح فورير فى صورته المختصرة المتكررة والمستخدم على نطـــاق واســع فى المتممات الرقمية للاعتماد عليه بشكل أساسى فى خوارزم قياس التردد وقيمة المتجه للإشـــارات الكهربيـــة المعبرة عن جهد وتيارات الشبكة. وكان الدافع الأساسى لهذه الدراسة التناقض الواضح ما بين التوصيـــات المختلفة للأبحاث العلمية المتقدمة على هذه المقالة والتى يتباين فيها التوصية باستخدام خوارزم قياس الـــتردد المبنية على مرشح فورير أو استخدام النظم القديمة المعتمدة على القياس الدقيق للحظات مرور الإشارة بالصفر أو استخدام النظم الحديثة مثل طرق فصل الموجات الحاملة والتى اعتبرت مثل هذه الطـــرق القـــديم منـــها والحديث أفضل من الطريقة المعتمدة على مرشح فورير. هذا مع العلم بأن الطريقة المعتمدة على مرشح فورير تعتبر الطريقة المثلى لما لها عبء حسابي إضافي بسيط على الميكروبروسيسور وتوفيرها فى كم الدوائر المتكاملة للمتمم. هذا بالإضافة لأن ما نشر من خصائص مرشح فورير كمقياس للمتجه اعتمد على الصورة المتواليـــة وعمم النتائج لتشمل الصورة المختصرة التكرارية بالإضافة إلى غياب القياسات المعملية فى معظم الدراسات.

ولقد قدمت المقالة دراسة مستفيضة ذات صبغة معملية أساسا باستخدام تكنولوجيا المعالجات الدقيقـــة ذات الأرقام العشرية وذلك لقياس وتحليل أداء مقياسى التردد ومتجه الإشارات تحت ظروف إشـــارات دخـــل متنوعة تماثل إشارات الجهد والتيار المتواجدة بمنظومة القوى الكهربية فى ظروف التشغيل والأخطاء العتـــادة. كما سجلت المقالة نتائج مهمة لاحتمال أن يتنامى الخطأ فى قيمة إشارة الدخل المقاسة بمرشح فورير المختصر خصوصا مع انحراف تردد الإشارة عن ٥٠ ذ/ث والذى يمكن أن يؤدى إلى التشغيل الخاطئ للمتمم. كمـــا اقترحت المقالة شكلا جديدا لتطبيق مرشح فورير يجمع ما بين الحجم المحدود من العمليات الحسابية للصـــورة المختصرة التكرارية والأداء المستقر للصورة المتوالية وذلك بعبء حسابى إضافى محدود للغاية.

كما سجلت النتائج المعملية أداءا متميزا لخوارزم قياس التردد مادام التغير فى التردد من قيمة إلى قيمة لحظيـــا أما إذا كان التغير ديناميكيا فإن الخوارزم يبتعد تماما عن دقة القياس ويفقد الكثير من حساسيته إلى أن يستقر عند قيمة تردد جديدة فتعود إلية دقته. وبالتالى تم استبيان تباين توصيات المقالات العلمية لهـــذا الخـــوارزم لاختلافهم فى اسلوب تقييمه. وقد أوصت المقالة بمزيد من الدراسة لخوارزم التردد لزيـــادة فعاليتـــه أثنـــاء التغيرات الديناميكية للتردد وذلك باستخدام إحدى طرق نظم الذكاء الاصطناعى.